Freescale Semiconductor
Data Sheet: Technical Data

Document Number: DSP56366
Rev. 3.1, 1/2007

DSP56366

24-Bit Audio Digital Signal Processor

1 Overview

The DSP56366 supports digital audio applications requiring sound field processing, acoustic equalization, and other digital audio algorithms. The DSP56366 uses the high performance, single-clock-per-cycle DSP56300 core family of programmable CMOS digital signal processors (DSPs) combined with the audio signal processing capability of the Freescale Symphony™ DSP family, as shown in Figure 1-1. This design provides a two-fold performance increase over Freescale's popular 56000 Symphony family of DSPs while retaining code compatibility. Significant architectural enhancements include a barrel shifter, 24-bit addressing, instruction cache, and direct memory access (DMA). The DSP56366 offers 120 million instructions per second (MIPS) using an internal 120 MHz clock at 3.3 V.

Contents

freescale™ semiconductor

Data Sheet Conventions

This data sheet uses the following conventions:

$\overline{\text{OVERBAR}}$	Used to indicate a signal that is active when pulled low (For example, the $\overline{\text{RESET}}$ pin is active when low.)
"asserted"	Means that a high true (active high) signal is high or that a low true (active low) signal is low
"deasserted"	Means that a high true (active high) signal is low or that a low true (active low) signal is high

Examples:	Signal/Symbol	Logic State	Signal State	Voltage*
	$\overline{\text{PIN}}$	True	Asserted	V_{IL} / V_{OL}
	$\overline{\text{PIN}}$	False	Deasserted	V_{IH} / V_{OH}
	PIN	True	Asserted	V_{IH} / V_{OH}
	PIN	False	Deasserted	V_{IL} / V_{OL}

Note: *Values for V_{IL}, V_{OL}, V_{IH}, and V_{OH} are defined by individual product specifications.

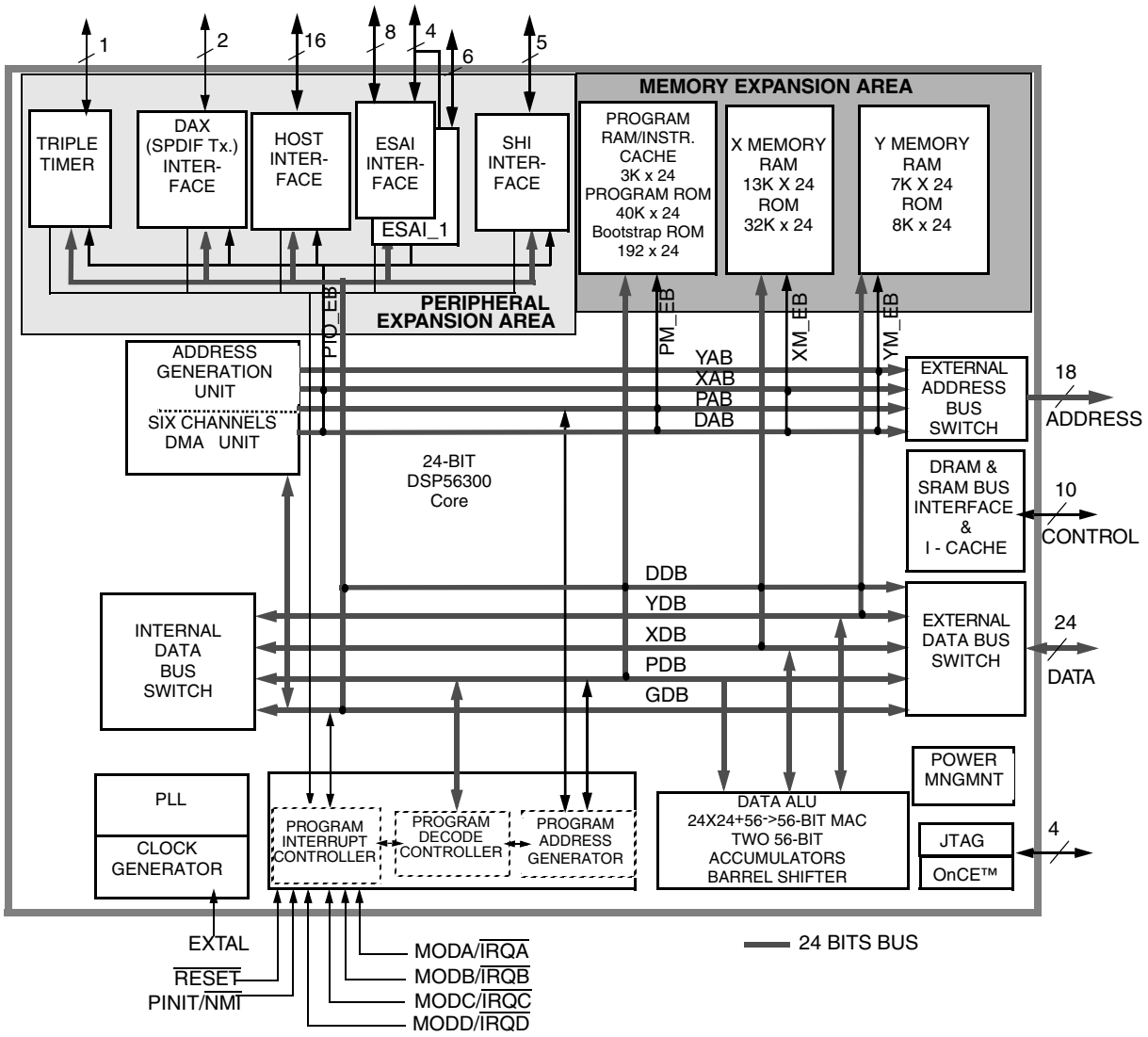


Figure 1-1 DSP56366 Block Diagram

1.1 Features

1.1.1 DSP56300 Modular Chassis

- 120 Million Instructions Per Second (MIPS) with an 120 MHz clock at 3.3V.
- Object Code Compatible with the 56K core.
- Data ALU with a 24 x 24 bit multiplier-accumulator and a 56-bit barrel shifter. 16-bit arithmetic support.
- Program Control with position independent code support and instruction cache support.
- Six-channel DMA controller.
- PLL based clocking with a wide range of frequency multiplications (1 to 4096), predivider factors (1 to 16) and power saving clock divider (2^i: i=0 to 7). Reduces clock noise.
- Internal address tracing support and OnCE™ for Hardware/Software debugging.
- JTAG port.
- Very low-power CMOS design, fully static design with operating frequencies down to DC.
- STOP and WAIT low-power standby modes.

1.1.2 On-chip Memory Configuration

- 7Kx24 Bit Y-Data RAM and 8Kx24 Bit Y-Data ROM.
- 13Kx24 Bit X-Data RAM and 32Kx24 Bit X-Data ROM.
- 40Kx24 Bit Program ROM.
- 3Kx24 Bit Program RAM and 192x24 Bit Bootstrap ROM. 1K of Program RAM may be used as Instruction Cache or for Program ROM patching.
- 2Kx24 Bit from Y Data RAM and 5Kx24 Bit from X Data RAM can be switched to Program RAM resulting in up to 10Kx24 Bit of Program RAM.

1.1.3 Off-chip Memory Expansion

- External Memory Expansion Port.
- Off-chip expansion up to two 16M x 24-bit word of Data memory.
- Off-chip expansion up to 16M x 24-bit word of Program memory.
- Simultaneous glueless interface to SRAM and DRAM.

1.1.4 Peripheral Modules

- Serial Audio Interface (ESAI): up to 4 receivers and up to 6 transmitters, master or slave. I^2S, Sony, AC97, network and other programmable protocols.
- Serial Audio Interface I(ESAI_1): up to 4 receivers and up to 6 transmitters, master or slave. I^2S, Sony, AC97, network and other programmable protocols
  The ESAI_1 shares four of the data pins with ESAI, and ESAI_1 does NOT support HCKR and HCKT (high frequency clocks)

- Serial Host Interface (SHI): SPI and I^2C protocols, multi master capability, 10-word receive FIFO, support for 8, 16 and 24-bit words.
- Byte-wide parallel Host Interface (HDI08) with DMA support.
- Triple Timer module (TEC).
- Digital Audio Transmitter (DAX): 1 serial transmitter capable of supporting the SPDIF, IEC958, CP-340 and AES/EBU digital audio formats.
- Pins of unused peripherals (except SHI) may be programmed as GPIO lines.

1.1.5 Packaging

- 144-pin plastic LQFP package.

1.2 Documentation

Table 1-1 lists the documents that provide a complete description of the DSP56366 and are required to design properly with the part. Documentation is available from a local Freescale distributor, a Freescale semiconductor sales office, a Freescale Literature Distribution Center, or through the Freescale DSP home page on the Internet (the source for the latest information).

Table 1-1 DSP56366 Documentation

Document Name	Description	Order Number
DSP56300 Family Manual	Detailed description of the 56300-family architecture and the 24-bit core processor and instruction set	DSP56300FM
DSP56366 User's Manual	Detailed description of memory, peripherals, and interfaces	DSP56366UM
DSP56366 Product Brief	Brief description of the chip	DSP56366P
DSP56366 Technical Data Sheet (this document)	Electrical and timing specifications; pin and package descriptions	DSP56366
IBIS Model	Input Output Buffer Information Specification.	For software or simulation models, contact sales or go to www.freescale.com.

2 Signal/Connection Descriptions

2.1 Signal Groupings

The input and output signals of the DSP56366 are organized into functional groups, which are listed in Table 2-1 and illustrated in Figure 2-1.

The DSP56366 is operated from a 3.3 V supply; however, some of the inputs can tolerate 5 V. A special notice for this feature is added to the signal descriptions of those inputs.

Table 2-1 DSP56366 Functional Signal Groupings

Functional Group		Number of Signals	Detailed Description
Power (V_{CC})		20	Table 2-2
Ground (GND)		18	Table 2-3
Clock and PLL		3	Table 2-4
Address bus	Port A[1]	18	Table 2-5
Data bus		24	Table 2-6
Bus control		10	Table 2-7
Interrupt and mode control		5	Table 2-8
HDI08	Port B[2]	16	Table 2-9
SHI		5	Table 2-10
ESAI	Port C[3]	12	Table 2-11
ESAI_1	Port E[4]	6	Table 2-12
Digital audio transmitter (DAX)	Port D[5]	2	Table 2-13
Timer		1	Table 2-14
JTAG/OnCE Port		4	Table 2-15

1 Port A is the external memory interface port, including the external address bus, data bus, and control signals.
2 Port B signals are the GPIO port signals which are multiplexed with the HDI08 signals.
3 Port C signals are the GPIO port signals which are multiplexed with the ESAI signals.
4 Port E signals are the GPIO port signals which are multiplexed with the ESAI_1 signals.
5 Port D signals are the GPIO port signals which are multiplexed with the DAX signals.

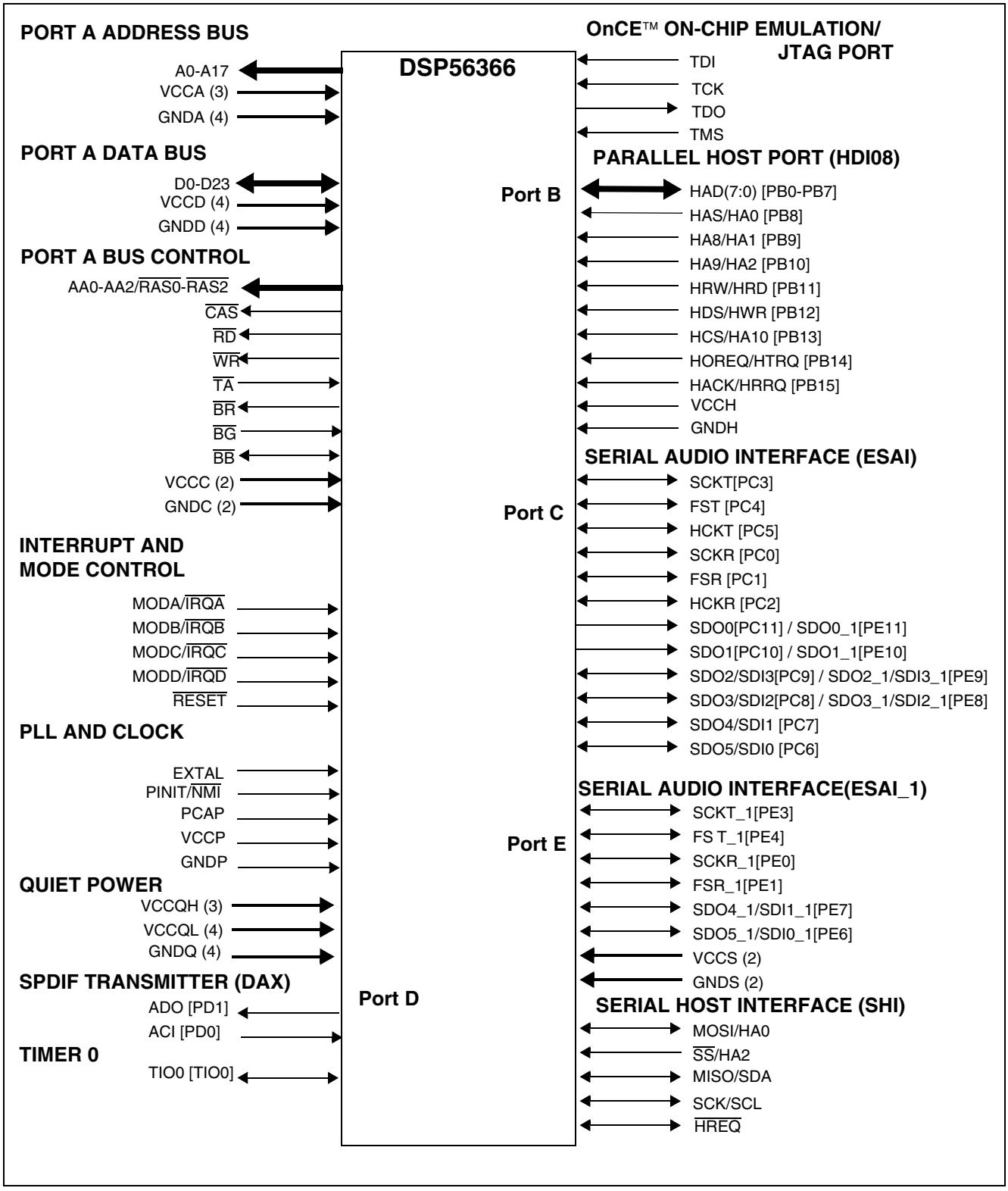


Figure 2-1 Signals Identified by Functional Group

2.2 Power

Table 2-2 Power Inputs

Power Name	Description
V_{CCP}	**PLL Power**—V_{CCP} is V_{CC} dedicated for PLL use. The voltage should be well-regulated and the input should be provided with an extremely low impedance path to the V_{CC} power rail. There is one V_{CCP} input.
V_{CCQL} (4)	**Quiet Core (Low) Power—**V_{CCQL} is an isolated power for the internal processing logic. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There are four V_{CCQL} inputs.
V_{CCQH} (3)	**Quiet External (High) Power**—V_{CCQH} is a quiet power source for I/O lines. This input must be tied externally to all other chip power inputs. The user must provide adequate decoupling capacitors. There are three V_{CCQH} inputs.
V_{CCA} (3)	**Address Bus Power**—V_{CCA} is an isolated power for sections of the address bus I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There are three V_{CCA} inputs.
V_{CCD} (4)	**Data Bus Power**—V_{CCD} is an isolated power for sections of the data bus I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There are four V_{CCD} inputs.
V_{CCC} (2)	**Bus Control Power**—V_{CCC} is an isolated power for the bus control I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There are two V_{CCC} inputs.
V_{CCH}	**Host Power**—V_{CCH} is an isolated power for the HDI08 I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There is one V_{CCH} input.
V_{CCS} (2)	**SHI, ESAI, ESAI_1, DAX and Timer Power** —V_{CCS} is an isolated power for the SHI, ESAI, ESAI_1, DAX and Timer. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors. There are two V_{CCS} inputs.

2.3 Ground

Table 2-3 Grounds

Ground Name	Description
GND_P	**PLL Ground**—GND_P is a ground dedicated for PLL use. The connection should be provided with an extremely low-impedance path to ground. V_{CCP} should be bypassed to GND_P by a 0.47 μF capacitor located as close as possible to the chip package. There is one GND_P connection.
GND_Q (4)	**Quiet Ground**—GND_Q is an isolated ground for the internal processing logic. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There are four GND_Q connections.
GND_A (4)	**Address Bus Ground**—GND_A is an isolated ground for sections of the address bus I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There are four GND_A connections.

Table 2-3 Grounds (continued)

Ground Name	Description
GND_D (4)	**Data Bus Ground**—GND_D is an isolated ground for sections of the data bus I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There are four GND_D connections.
GND_C (2)	**Bus Control Ground**—GND_C is an isolated ground for the bus control I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There are two GND_C connections.
GND_H	**Host Ground**—GND_h is an isolated ground for the HD08 I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There is one GND_H connection.
GND_S (2)	**SHI, ESAI, ESAI_1, DAX and Timer Ground**—GND_S is an isolated ground for the SHI, ESAI, ESAI_1, DAX and Timer. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors. There are two GND_S connections.

2.4 Clock and PLL

Table 2-4 Clock and PLL Signals

Signal Name	Type	State during Reset	Signal Description
EXTAL	Input	Input	**External Clock Input**—An external clock source must be connected to EXTAL in order to supply the clock to the internal clock generator and PLL. *This input cannot tolerate 5 V.*
PCAP	Input	Input	**PLL Capacitor**—PCAP is an input connecting an off-chip capacitor to the PLL filter. Connect one capacitor terminal to PCAP and the other terminal to V_{CCP}. If the PLL is not used, PCAP may be tied to V_{CC}, GND, or left floating.
PINIT/$\overline{\text{NMI}}$	Input	Input	**PLL Initial/Nonmaskable Interrupt**—During assertion of $\overline{\text{RESET}}$, the value of PINIT/$\overline{\text{NMI}}$ is written into the PLL Enable (PEN) bit of the PLL control register, determining whether the PLL is enabled or disabled. After $\overline{\text{RESET}}$ de assertion and during normal instruction processing, the PINIT/$\overline{\text{NMI}}$ Schmitt-trigger input is a negative-edge-triggered nonmaskable interrupt (NMI) request internally synchronized to internal system clock. *This input cannot tolerate 5 V.*

2.5 External Memory Expansion Port (Port A)

When the DSP56366 enters a low-power standby mode (stop or wait), it releases bus mastership and tri-states the relevant port A signals: A0–A17, D0–D23, AA0/$\overline{\text{RAS0}}$–AA2/$\overline{\text{RAS2}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{BB}}$, $\overline{\text{CAS}}$.

2.5.1 External Address Bus

Table 2-5 External Address Bus Signals

Signal Name	Type	State during Reset	Signal Description
A0–A17	Output	Tri-stated	**Address Bus**—When the DSP is the bus master, A0–A17 are active-high outputs that specify the address for external program and data memory accesses. Otherwise, the signals are tri-stated. To minimize power dissipation, A0–A17 do not change state when external memory spaces are not being accessed.

2.5.2 External Data Bus

Table 2-6 External Data Bus Signals

Signal Name	Type	State during Reset	Signal Description
D0–D23	Input/Output	Tri-stated	**Data Bus**—When the DSP is the bus master, D0–D23 are active-high, bidirectional input/outputs that provide the bidirectional data bus for external program and data memory accesses. Otherwise, D0–D23 are tri-stated.

2.5.3 External Bus Control

Table 2-7 External Bus Control Signals

Signal Name	Type	State during Reset	Signal Description
AA0–AA2/ $\overline{\text{RAS0}}$–$\overline{\text{RAS2}}$	Output	Tri-stated	**Address Attribute or Row Address Strobe**—When defined as AA, these signals can be used as chip selects or additional address lines. When defined as $\overline{\text{RAS}}$, these signals can be used as $\overline{\text{RAS}}$ for DRAM interface. These signals are tri-statable outputs with programmable polarity.
$\overline{\text{CAS}}$	Output	Tri-stated	**Column Address Strobe**— When the DSP is the bus master, $\overline{\text{CAS}}$ is an active-low output used by DRAM to strobe the column address. Otherwise, if the bus mastership enable (BME) bit in the DRAM control register is cleared, the signal is tri-stated.
$\overline{\text{RD}}$	Output	Tri-stated	**Read Enable**—When the DSP is the bus master, $\overline{\text{RD}}$ is an active-low output that is asserted to read external memory on the data bus (D0-D23). Otherwise, $\overline{\text{RD}}$ is tri-stated.
$\overline{\text{WR}}$	Output	Tri-stated	**Write Enable**—When the DSP is the bus master, $\overline{\text{WR}}$ is an active-low output that is asserted to write external memory on the data bus (D0-D23). Otherwise, $\overline{\text{WR}}$ is tri-stated.

Table 2-7 External Bus Control Signals (continued)

Signal Name	Type	State during Reset	Signal Description
$\overline{TA}$	Input	Ignored Input	**Transfer Acknowledge**—If the DSP is the bus master and there is no external bus activity, or the DSP is not the bus master, the $\overline{TA}$ input is ignored. The $\overline{TA}$ input is a data transfer acknowledge (DTACK) function that can extend an external bus cycle indefinitely. Any number of wait states (1, 2. . .infinity) may be added to the wait states inserted by the BCR by keeping $\overline{TA}$ deasserted. In typical operation, $\overline{TA}$ is deasserted at the start of a bus cycle, is asserted to enable completion of the bus cycle, and is deasserted before the next bus cycle. The current bus cycle completes one clock period after $\overline{TA}$ is asserted synchronous to the internal system clock. The number of wait states is determined by the $\overline{TA}$ input or by the bus control register (BCR), whichever is longer. The BCR can be used to set the minimum number of wait states in external bus cycles. In order to use the $\overline{TA}$ functionality, the BCR must be programmed to at least one wait state. A zero wait state access cannot be extended by $\overline{TA}$ deassertion, otherwise improper operation may result. $\overline{TA}$ can operate synchronously or asynchronously, depending on the setting of the TAS bit in the operating mode register (OMR). $\overline{TA}$ functionality may not be used while performing DRAM type accesses, otherwise improper operation may result.
$\overline{BR}$	Output	Output (deasserted)	**Bus Request**—$\overline{BR}$ is an active-low output, never tri-stated. $\overline{BR}$ is asserted when the DSP requests bus mastership. $\overline{BR}$ is deasserted when the DSP no longer needs the bus. $\overline{BR}$ may be asserted or deasserted independent of whether the DSP56366 is a bus master or a bus slave. Bus “parking” allows $\overline{BR}$ to be deasserted even though the DSP56366 is the bus master. (See the description of bus “parking” in the $\overline{BB}$ signal description.) The bus request hold (BRH) bit in the BCR allows $\overline{BR}$ to be asserted under software control even though the DSP does not need the bus. $\overline{BR}$ is typically sent to an external bus arbitrator that controls the priority, parking, and tenure of each master on the same external bus. $\overline{BR}$ is only affected by DSP requests for the external bus, never for the internal bus. During hardware reset, $\overline{BR}$ is deasserted and the arbitration is reset to the bus slave state.

Table 2-7 External Bus Control Signals (continued)

Signal Name	Type	State during Reset	Signal Description
$\overline{BG}$	Input	Ignored Input	**Bus Grant**—$\overline{BG}$ is an active-low input. $\overline{BG}$ is asserted by an external bus arbitration circuit when the DSP56366 becomes the next bus master. When $\overline{BG}$ is asserted, the DSP56366 must wait until $\overline{BB}$ is deasserted before taking bus mastership. When $\overline{BG}$ is deasserted, bus mastership is typically given up at the end of the current bus cycle. This may occur in the middle of an instruction that requires more than one external bus cycle for execution. For proper $\overline{BG}$ operation, the asynchronous bus arbitration enable bit (ABE) in the OMR register must be set.
$\overline{BB}$	Input/Output	Input	**Bus Busy**—$\overline{BB}$ is a bidirectional active-low input/output. $\overline{BB}$ indicates that the bus is active. Only after $\overline{BB}$ is deasserted can the pending bus master become the bus master (and then assert the signal again). The bus master may keep $\overline{BB}$ asserted after ceasing bus activity regardless of whether $\overline{BR}$ is asserted or deasserted. This is called “bus parking” and allows the current bus master to reuse the bus without rearbitration until another device requires the bus. The deassertion of $\overline{BB}$ is done by an “active pull-up” method (i.e., $\overline{BB}$ is driven high and then released and held high by an external pull-up resistor). For proper $\overline{BB}$ operation, the asynchronous bus arbitration enable bit (ABE) in the OMR register must be set. $\overline{BB}$ requires an external pull-up resistor.

2.6 Interrupt and Mode Control

The interrupt and mode control signals select the chip's operating mode as it comes out of hardware reset. After RESET is deasserted, these inputs are hardware interrupt request lines.

Table 2-8 Interrupt and Mode Control

Signal Name	Type	State during Reset	Signal Description
MODA/IRQA	Input	Input	**Mode Select A/External Interrupt Request A—**MODA/IRQA is an active-low Schmitt-trigger input, internally synchronized to the DSP clock. MODA/IRQA selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into the OMR when the RESET signal is deasserted. If the processor is in the stop standby state and the MODA/IRQA pin is pulled to GND, the processor will exit the stop state. *This input is 5 V tolerant.*
MODB/IRQB	Input	Input	**Mode Select B/External Interrupt Request B—**MODB/IRQB is an active-low Schmitt-trigger input, internally synchronized to the DSP clock. MODB/IRQB selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into OMR when the RESET signal is deasserted. This input is 5 V tolerant.
MODC/IRQC	Input	Input	**Mode Select C/External Interrupt Request C—**MODC/IRQC is an active-low Schmitt-trigger input, internally synchronized to the DSP clock. MODC/IRQC selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into OMR when the RESET signal is deasserted. This input is 5 V tolerant.
MODD/IRQD	Input	Input	**Mode Select D/External Interrupt Request D**—MODD/IRQD is an active-low Schmitt-trigger input, internally synchronized to the DSP clock. MODD/IRQD selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into OMR when the RESET signal is deasserted. This input is 5 V tolerant.
RESET	Input	Input	**Reset—**RESET is an active-low, Schmitt-trigger input. When asserted, the chip is placed in the Reset state and the internal phase generator is reset. The Schmitt-trigger input allows a slowly rising input (such as a capacitor charging) to reset the chip reliably. When the RESET signal is deasserted, the initial chip operating mode is latched from the MODA, MODB, MODC, and MODD inputs. The RESET signal must be asserted during power up. A stable EXTAL signal must be supplied while RESET is being asserted. *This input is 5 V tolerant.*

2.7 Parallel Host Interface (HDI08)

The HDI08 provides a fast, 8-bit, parallel data port that may be connected directly to the host bus. The HDI08 supports a variety of standard buses and can be directly connected to a number of industry standard microcomputers, microprocessors, DSPs, and DMA hardware.

Table 2-9 Host Interface

Signal Name	Type	State during Reset	Signal Description
H0–H7	Input/ output	GPIO disconnected	**Host Data—**When HDI08 is programmed to interface a nonmultiplexed host bus and the HI function is selected, these signals are lines 0–7 of the bidirectional, tri-state data bus.
HAD0–HAD7	Input/ output	GPIO disconnected	**Host Address/Data—**When HDI08 is programmed to interface a multiplexed host bus and the HI function is selected, these signals are lines 0–7 of the address/data bidirectional, multiplexed, tri-state bus.
PB0–PB7	Input, output, or disconnected	GPIO disconnected	**Port B 0–7**—When the HDI08 is configured as GPIO, these signals are individually programmable as input, output, or internally disconnected.
			The default state after reset for these signals is GPIO disconnected. These inputs are 5 V tolerant.
HA0	Input	GPIO disconnected	**Host Address Input 0**—When the HDI08 is programmed to interface a nonmultiplexed host bus and the HI function is selected, this signal is line 0 of the host address input bus.
$\overline{\text{HAS}}$/HAS	Input	GPIO disconnected	**Host Address Strobe—**When HDI08 is programmed to interface a multiplexed host bus and the HI function is selected, this signal is the host address strobe (HAS) Schmitt-trigger input. The polarity of the address strobe is programmable, but is configured active-low ($\overline{\text{HAS}}$) following reset.
PB8	Input, output, or disconnected	GPIO disconnected	**Port B 8**—When the HDI08 is configured as GPIO, this signal is individually programmed as input, output, or internally disconnected. The default state after reset for this signal is GPIO disconnected. *This input is 5 V tolerant.*
HA1	Input	GPIO disconnected	**Host Address Input 1**—When the HDI08 is programmed to interface a nonmultiplexed host bus and the HI function is selected, this signal is line 1 of the host address (HA1) input bus.
HA8	Input	GPIO disconnected	**Host Address 8**—When HDI08 is programmed to interface a multiplexed host bus and the HI function is selected, this signal is line 8 of the host address (HA8) input bus.
PB9	Input, output, or disconnected	GPIO disconnected	**Port B 9**—When the HDI08 is configured as GPIO, this signal is individually programmed as input, output, or internally disconnected. The default state after reset for this signal is GPIO disconnected. This input is 5 V tolerant.

Table 2-9 Host Interface (continued)

Signal Name	Type	State during Reset	Signal Description
HA2	Input	GPIO disconnected	**Host Address Input 2**—When the HDI08 is programmed to interface a non-multiplexed host bus and the HI function is selected, this signal is line 2 of the host address (HA2) input bus.
HA9	Input	GPIO disconnected	**Host Address 9**—When HDI08 is programmed to interface a multiplexed host bus and the HI function is selected, this signal is line 9 of the host address (HA9) input bus.
PB10	Input, Output, or Disconnected	GPIO disconnected	**Port B 10**—When the HDI08 is configured as GPIO, this signal is individually programmed as input, output, or internally disconnected. The default state after reset for this signal is GPIO disconnected. *This input is 5 V tolerant.*
HRW	Input	GPIO disconnected	**Host Read/Write**—When HDI08 is programmed to interface a single-data-strobe host bus and the HI function is selected, this signal is the Host Read/$\overline{\text{Write}}$ (HRW) input.
$\overline{\text{HRD}}$/ HRD	Input	GPIO disconnected	**Host Read Data**—When HDI08 is programmed to interface a double-data-strobe host bus and the HI function is selected, this signal is the host read data strobe (HRD) Schmitt-trigger input. The polarity of the data strobe is programmable, but is configured as active-low ($\overline{\text{HRD}}$) after reset.
PB11	Input, Output, or Disconnected	GPIO disconnected	**Port B 11**—When the HDI08 is configured as GPIO, this signal is individually programmed as input, output, or internally disconnected. The default state after reset for this signal is GPIO disconnected. This input is 5 V tolerant.
$\overline{\text{HDS}}$/ HDS	Input	GPIO disconnected	**Host Data Strobe—**When HDI08 is programmed to interface a single-data-strobe host bus and the HI function is selected, this signal is the host data strobe (HDS) Schmitt-trigger input. The polarity of the data strobe is programmable, but is configured as active-low ($\overline{\text{HDS}}$) following reset.
$\overline{\text{HWR}}$/ HWR	Input	GPIO disconnected	**Host Write Data**—When HDI08 is programmed to interface a double-data-strobe host bus and the HI function is selected, this signal is the host write data strobe (HWR) Schmitt-trigger input. The polarity of the data strobe is programmable, but is configured as active-low ($\overline{\text{HWR}}$) following reset.
PB12	Input, output, or disconnected	GPIO disconnected	**Port B 12**—When the HDI08 is configured as GPIO, this signal is individually programmed as input, output, or internally disconnected. The default state after reset for this signal is GPIO disconnected. This input is 5 V tolerant.
HCS	Input	GPIO disconnected	**Host Chip Select—**When HDI08 is programmed to interface a nonmultiplexed host bus and the HI function is selected, this signal is the host chip select (HCS) input. The polarity of the chip select is programmable, but is configured active-low ($\overline{\text{HCS}}$) after reset.

Table 2-9 Host Interface (continued)

Signal Name	Type	State during Reset	Signal Description
HA10	Input	GPIO disconnected	**Host Address 10**—When HDI08 is programmed to interface a multiplexed host bus and the HI function is selected, this signal is line 10 of the host address (HA10) input bus.
PB13	Input, output, or disconnected	GPIO disconnected	**Port B 13**—When the HDI08 is configured as GPIO, this signal is individually programmed as input, output, or internally disconnected. The default state after reset for this signal is GPIO disconnected. This input is 5 V tolerant.
$\overline{\text{HOREQ}}$/ HOREQ	Output	GPIO disconnected	**Host Request**—When HDI08 is programmed to interface a single host request host bus and the HI function is selected, this signal is the host request (HOREQ) output. The polarity of the host request is programmable, but is configured as active-low ($\overline{\text{HOREQ}}$) following reset. The host request may be programmed as a driven or open-drain output.
$\overline{\text{HTRQ}}$/ HTRQ	Output	GPIO disconnected	**Transmit Host Request—**When HDI08 is programmed to interface a double host request host bus and the HI function is selected, this signal is the transmit host request (HTRQ) output. The polarity of the host request is programmable, but is configured as active-low ($\overline{\text{HTRQ}}$) following reset. The host request may be programmed as a driven or open-drain output.
PB14	Input, output, or disconnected	GPIO disconnected	**Port B 14**—When the HDI08 is configured as GPIO, this signal is individually programmed as input, output, or internally disconnected. The default state after reset for this signal is GPIO disconnected. This input is 5 V tolerant.
$\overline{\text{HACK}}$/ HACK	Input	GPIO disconnected	**Host Acknowledge**—When HDI08 is programmed to interface a single host request host bus and the HI function is selected, this signal is the host acknowledge (HACK) Schmitt-trigger input. The polarity of the host acknowledge is programmable, but is configured as active-low ($\overline{\text{HACK}}$) after reset.
$\overline{\text{HRRQ}}$/ HRRQ	Output	GPIO disconnected	**Receive Host Request**—When HDI08 is programmed to interface a double host request host bus and the HI function is selected, this signal is the receive host request (HRRQ) output. The polarity of the host request is programmable, but is configured as active-low ($\overline{\text{HRRQ}}$) after reset. The host request may be programmed as a driven or open-drain output.
PB15	Input, output, or disconnected	GPIO disconnected	**Port B 15**—When the HDI08 is configured as GPIO, this signal is individually programmed as input, output, or internally disconnected. The default state after reset for this signal is GPIO disconnected. *This input is 5 V tolerant.*

2.8 Serial Host Interface

The SHI has five I/O signals that can be configured to allow the SHI to operate in either SPI or I^2C mode.

Table 2-10 Serial Host Interface Signals

Signal Name	Signal Type	State during Reset	Signal Description
SCK	Input or output	Tri-stated	**SPI Serial Clock**—The SCK signal is an output when the SPI is configured as a master and a Schmitt-trigger input when the SPI is configured as a slave. When the SPI is configured as a master, the SCK signal is derived from the internal SHI clock generator. When the SPI is configured as a slave, the SCK signal is an input, and the clock signal from the external master synchronizes the data transfer. The SCK signal is ignored by the SPI if it is defined as a slave and the slave select ($\overline{SS}$) signal is not asserted. In both the master and slave SPI devices, data is shifted on one edge of the SCK signal and is sampled on the opposite edge where data is stable. Edge polarity is determined by the SPI transfer protocol.
SCL	Input or output	Tri-stated	**I^2C Serial Clock**—SCL carries the clock for I^2C bus transactions in the I^2C mode. SCL is a Schmitt-trigger input when configured as a slave and an open-drain output when configured as a master. SCL should be connected to V_{CC} through a pull-up resistor. This signal is tri-stated during hardware, software, and individual reset. Thus, there is no need for an external pull-up in this state. This input is 5 V tolerant.
MISO	Input or output	Tri-stated	**SPI Master-In-Slave-Out**—When the SPI is configured as a master, MISO is the master data input line. The MISO signal is used in conjunction with the MOSI signal for transmitting and receiving serial data. This signal is a Schmitt-trigger input when configured for the SPI Master mode, an output when configured for the SPI Slave mode, and tri-stated if configured for the SPI Slave mode when $\overline{SS}$ is deasserted. An external pull-up resistor is not required for SPI operation.
SDA	Input or open-drain output	Tri-stated	**I^2C Data and Acknowledge**—In I^2C mode, SDA is a Schmitt-trigger input when receiving and an open-drain output when transmitting. SDA should be connected to V_{CC} through a pull-up resistor. SDA carries the data for I^2C transactions. The data in SDA must be stable during the high period of SCL. The data in SDA is only allowed to change when SCL is low. When the bus is free, SDA is high. The SDA line is only allowed to change during the time SCL is high in the case of start and stop events. A high-to-low transition of the SDA line while SCL is high is a unique situation, and is defined as the start event. A low-to-high transition of SDA while SCL is high is a unique situation defined as the stop event. This signal is tri-stated during hardware, software, and individual reset. Thus, there is no need for an external pull-up in this state. This input is 5 V tolerant.
MOSI	Input or output	Tri-stated	**SPI Master-Out-Slave-In**—When the SPI is configured as a master, MOSI is the master data output line. The MOSI signal is used in conjunction with the MISO signal for transmitting and receiving serial data. MOSI is the slave data input line when the SPI is configured as a slave. This signal is a Schmitt-trigger input when configured for the SPI Slave mode.

Table 2-10 Serial Host Interface Signals (continued)

Signal Name	Signal Type	State during Reset	Signal Description
HA0	Input		**I²C Slave Address 0**—This signal uses a Schmitt-trigger input when configured for the I²C mode. When configured for I²C slave mode, the HA0 signal is used to form the slave device address. HA0 is ignored when configured for the I²C master mode. This signal is tri-stated during hardware, software, and individual reset. Thus, there is no need for an external pull-up in this state. This input is 5 V tolerant.
$\overline{SS}$	Input	Tri-stated	**SPI Slave Select**—This signal is an active low Schmitt-trigger input when configured for the SPI mode. When configured for the SPI Slave mode, this signal is used to enable the SPI slave for transfer. When configured for the SPI master mode, this signal should be kept deasserted (pulled high). If it is asserted while configured as SPI master, a bus error condition is flagged. If $\overline{SS}$ is deasserted, the SHI ignores SCK clocks and keeps the MISO output signal in the high-impedance state.
HA2	Input		**I²C Slave Address 2**—This signal uses a Schmitt-trigger input when configured for the I²C mode. When configured for the I²C Slave mode, the HA2 signal is used to form the slave device address. HA2 is ignored in the I²C master mode. This signal is tri-stated during hardware, software, and individual reset. Thus, there is no need for an external pull-up in this state. *This input is 5 V tolerant*.
$\overline{HREQ}$	Input or Output	Tri-stated	**Host Request**—This signal is an active low Schmitt-trigger input when configured for the master mode but an active low output when configured for the slave mode. When configured for the slave mode, $\overline{HREQ}$ is asserted to indicate that the SHI is ready for the next data word transfer and deasserted at the first clock pulse of the new data word transfer. When configured for the master mode, $\overline{HREQ}$ is an input. When asserted by the external slave device, it will trigger the start of the data word transfer by the master. After finishing the data word transfer, the master will await the next assertion of $\overline{HREQ}$ to proceed to the next transfer. This signal is tri-stated during hardware, software, personal reset, or when the HREQ1–HREQ0 bits in the HCSR are cleared. There is no need for external pull-up in this state. *This input is 5 V toler*ant.

2.9 Enhanced Serial Audio Interface

Table 2-11 Enhanced Serial Audio Interface Signals

Signal Name	Signal Type	State during Reset	Signal Description
HCKR	Input or output	GPIO disconnected	**High Frequency Clock for Receiver**—When programmed as an input, this signal provides a high frequency clock source for the ESAI receiver as an alternate to the DSP core clock. When programmed as an output, this signal can serve as a high-frequency sample clock (e.g., for external digital to analog converters [DACs]) or as an additional system clock.
PC2	Input, output, or disconnected	GPIO disconnected	**Port C 2**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. *This input is 5 V tolerant.*
HCKT	Input or output	GPIO disconnected	**High Frequency Clock for Transmitter**—When programmed as an input, this signal provides a high frequency clock source for the ESAI transmitter as an alternate to the DSP core clock. When programmed as an output, this signal can serve as a high frequency sample clock (e.g., for external DACs) or as an additional system clock.
PC5	Input, output, or disconnected	GPIO disconnected	**Port C 5**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 5 V tolerant.
FSR	Input or output	GPIO disconnected	**Frame Sync for Receiver**—This is the receiver frame sync input/output signal. In the asynchronous mode (SYN=0), the FSR pin operates as the frame sync input or output used by all the enabled receivers. In the synchronous mode (SYN=1), it operates as either the serial flag 1 pin (TEBE=0), or as the transmitter external buffer enable control (TEBE=1, RFSD=1). When this pin is configured as serial flag pin, its direction is determined by the RFSD bit in the RCCR register. When configured as the output flag OF1, this pin will reflect the value of the OF1 bit in the SAICR register, and the data in the OF1 bit will show up at the pin synchronized to the frame sync in normal mode or the slot in network mode. When configured as the input flag IF1, the data value at the pin will be stored in the IF1 bit in the SAISR register, synchronized by the frame sync in normal mode or the slot in network mode.
PC1	Input, output, or disconnected	GPIO disconnected	**Port C 1**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 5 V tolerant.

Table 2-11 Enhanced Serial Audio Interface Signals (continued)

Signal Name	Signal Type	State during Reset	Signal Description
FST	Input or output	GPIO disconnected	**Frame Sync for Transmitter**—This is the transmitter frame sync input/output signal. For synchronous mode, this signal is the frame sync for both transmitters and receivers. For asynchronous mode, FST is the frame sync for the transmitters only. The direction is determined by the transmitter frame sync direction (TFSD) bit in the ESAI transmit clock control register (TCCR).
PC4	Input, output, or disconnected		**Port C 4**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 5 V tolerant.
SCKR	Input or output	GPIO disconnected	**Receiver Serial Clock**—SCKR provides the receiver serial bit clock for the ESAI. The SCKR operates as a clock input or output used by all the enabled receivers in the asynchronous mode (SYN=0), or as serial flag 0 pin in the synchronous mode (SYN=1). When this pin is configured as serial flag pin, its direction is determined by the RCKD bit in the RCCR register. When configured as the output flag OF0, this pin will reflect the value of the OF0 bit in the SAICR register, and the data in the OF0 bit will show up at the pin synchronized to the frame sync in normal mode or the slot in network mode. When configured as the input flag IF0, the data value at the pin will be stored in the IF0 bit in the SAISR register, synchronized by the frame sync in normal mode or the slot in network mode.
PC0	Input, output, or disconnected	GPIO disconnected	**Port C 0**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 5 V tolerant.
SCKT	Input or output	GPIO disconnected	**Transmitter Serial Clock**—This signal provides the serial bit rate clock for the ESAI. SCKT is a clock input or output used by all enabled transmitters and receivers in synchronous mode, or by all enabled transmitters in asynchronous mode.
PC3	Input, output, or disconnected	GPIO disconnected	**Port C 3**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 5 V tolerant.
SDO5	Output	GPIO disconnected	**Serial Data Output 5**—When programmed as a transmitter, SDO5 is used to transmit data from the TX5 serial transmit shift register.
SDI0	Input	GPIO disconnected	**Serial Data Input 0**—When programmed as a receiver, SDI0 is used to receive serial data into the RX0 serial receive shift register.

Table 2-11 Enhanced Serial Audio Interface Signals (continued)

Signal Name	Signal Type	State during Reset	Signal Description
PC6	Input, output, or disconnected	GPIO disconnected	**Port C 6**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 5 V tolerant.
SDO4	Output	GPIO disconnected	**Serial Data Output 4**—When programmed as a transmitter, SDO4 is used to transmit data from the TX4 serial transmit shift register.
SDI1	Input	GPIO disconnected	**Serial Data Input 1**—When programmed as a receiver, SDI1 is used to receive serial data into the RX1 serial receive shift register.
PC7	Input, output, or disconnected	GPIO disconnected	**Port C 7**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 5 V tolerant.
SDO3/SDO3_1	Output	GPIO disconnected	**Serial Data Output 3**—When programmed as a transmitter, SDO3 is used to transmit data from the TX3 serial transmit shift register. When enabled for ESAI_1 operation, this is the ESAI_1 Serial Data Output 3.
SDI2/ SDI2_1	Input	GPIO disconnected	**Serial Data Input 2**—When programmed as a receiver, SDI2 is used to receive serial data into the RX2 serial receive shift register. When enabled for ESAI_1 operation, this is the ESAI_1 Serial Data Input 2.
PC8/PE8	Input, output, or disconnected	GPIO disconnected	**Port C 8**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. When enabled for ESAI_1 GPIO, this is the Port E 8 signal. The default state after reset is GPIO disconnected. This input is 5 V tolerant.
SDO2/ SDO2_1	Output	GPIO disconnected	**Serial Data Output 2**—When programmed as a transmitter, SDO2 is used to transmit data from the TX2 serial transmit shift register. When enabled for ESAI_1 operation, this is the ESAI_1 Serial Data Output 2.
SDI3/SDI3_1	Input	GPIO disconnected	**Serial Data Input 3**—When programmed as a receiver, SDI3 is used to receive serial data into the RX3 serial receive shift register. When enabled for ESAI_1 operation, this is the ESAI_1 Serial Data Input 3.
PC9/PE9	Input, output, or disconnected	GPIO disconnected	**Port C 9**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. When enabled for ESAI_1 GPIO, this is the Port E 9 signal. The default state after reset is GPIO disconnected. This input is 5 V tolerant.

Table 2-11 Enhanced Serial Audio Interface Signals (continued)

Signal Name	Signal Type	State during Reset	Signal Description
SDO1/ SDO1_1	Output	GPIO disconnected	**Serial Data Output 1**—SDO1 is used to transmit data from the TX1 serial transmit shift register. When enabled for ESAI_1 operation, this is the ESAI_1 Serial Data Output 1.
PC10/ PE10	Input, output, or disconnected	GPIO disconnected	**Port C 10**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. When enabled for ESAI_1 GPIO, this is the Port E 10 signal. The default state after reset is GPIO disconnected. This input is 5 V tolerant.
SDO0/SDO0_1	Output	GPIO disconnected	**Serial Data Output 0**—SDO0 is used to transmit data from the TX0 serial transmit shift register. When enabled for ESAI_1 operation, this is the ESAI_1 Serial Data Output 0.
PC11/ PE11	Input, output, or disconnected	GPIO disconnected	**Port C 11**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. When enabled for ESAI_1 GPIO, this is the Port E 11 signal. The default state after reset is GPIO disconnected. This input is 5 V tolerant.

2.10 Enhanced Serial Audio Interface_1

Table 2-12 Enhanced Serial Audio Interface_1 Signals

Signal Name	Signal Type	State during Reset	Signal Description
FSR_1	Input or output	GPIO disconnected	**Frame Sync for Receiver_1**—This is the receiver frame sync input/output signal. In the asynchronous mode (SYN=0), the FSR pin operates as the frame sync input or output used by all the enabled receivers. In the synchronous mode (SYN=1), it operates as either the serial flag 1 pin (TEBE=0), or as the transmitter external buffer enable control (TEBE=1, RFSD=1). When this pin is configured as serial flag pin, its direction is determined by the RFSD bit in the RCCR register. When configured as the output flag OF1, this pin will reflect the value of the OF1 bit in the SAICR register, and the data in the OF1 bit will show up at the pin synchronized to the frame sync in normal mode or the slot in network mode. When configured as the input flag IF1, the data value at the pin will be stored in the IF1 bit in the SAISR register, synchronized by the frame sync in normal mode or the slot in network mode.
PE1	Input, output, or disconnected	GPIO disconnected	**Port E 1**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input cannot tolerate 5 V.
FST_1	Input or output	GPIO disconnected	**Frame Sync for Transmitter_1**—This is the transmitter frame sync input/output signal. For synchronous mode, this signal is the frame sync for both transmitters and receivers. For asynchronous mode, FST is the frame sync for the transmitters only. The direction is determined by the transmitter frame sync direction (TFSD) bit in the ESAI transmit clock control register (TCCR).
PE4	Input, output, or disconnected	GPIO disconnected	**Port E 4**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input cannot tolerate 5 V.
SCKR_1	Input or output	GPIO disconnected	**Receiver Serial Clock_1**—SCKR provides the receiver serial bit clock for the ESAI. The SCKR operates as a clock input or output used by all the enabled receivers in the asynchronous mode (SYN=0), or as serial flag 0 pin in the synchronous mode (SYN=1). When this pin is configured as serial flag pin, its direction is determined by the RCKD bit in the RCCR register. When configured as the output flag OF0, this pin will reflect the value of the OF0 bit in the SAICR register, and the data in the OF0 bit will show up at the pin synchronized to the frame sync in normal mode or the slot in network mode. When configured as the input flag IF0, the data value at the pin will be stored in the IF0 bit in the SAISR register, synchronized by the frame sync in normal mode or the slot in network mode.

Table 2-12 Enhanced Serial Audio Interface_1 Signals

Signal Name	Signal Type	State during Reset	Signal Description
PE0	Input, output, or disconnected	GPIO disconnected	**Port E 0**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input cannot tolerate 5 V.
SCKT_1	Input or output	GPIO disconnected	**Transmitter Serial Clock_1**—This signal provides the serial bit rate clock for the ESAI. SCKT is a clock input or output used by all enabled transmitters and receivers in synchronous mode, or by all enabled transmitters in asynchronous mode.
PE3	Input, output, or disconnected	GPIO disconnected	**Port E 3**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input cannot tolerate 5 V.
SDO5_1	Output	GPIO disconnected	**Serial Data Output 5_1**—When programmed as a transmitter, SDO5 is used to transmit data from the TX5 serial transmit shift register.
SDI0_1	Input	GPIO disconnected	**Serial Data Input 0_1**—When programmed as a receiver, SDI0 is used to receive serial data into the RX0 serial receive shift register.
PE6	Input, output, or disconnected	GPIO disconnected	**Port E 6**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input cannot tolerate 5 V.
SDO4_1	Output	GPIO disconnected	**Serial Data Output 4_1**—When programmed as a transmitter, SDO4 is used to transmit data from the TX4 serial transmit shift register.
SDI1_1	Input	GPIO disconnected	**Serial Data Input 1_1**—When programmed as a receiver, SDI1 is used to receive serial data into the RX1 serial receive shift register.
PE7	Input, output, or disconnected	GPIO disconnected	**Port E 7**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 5 V tolerant.

2.11 SPDIF Transmitter Digital Audio Interface

Table 2-13 Digital Audio Interface (DAX) Signals

Signal Name	Type	State During Reset	Signal Description
ACI	Input	GPIO Disconnected	**Audio Clock Input**—This is the DAX clock input. When programmed to use an external clock, this input supplies the DAX clock. The external clock frequency must be 256, 384, or 512 times the audio sampling frequency (256 × Fs, 384 × Fs or 512 × Fs, respectively).
PD0	Input, output, or disconnected	GPIO Disconnected	**Port D 0**—When the DAX is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 5 V tolerant.
ADO	Output	GPIO Disconnected	**Digital Audio Data Output**—This signal is an audio and non-audio output in the form of AES/EBU, CP340 and IEC958 data in a biphase mark format.
PD1	Input, output, or disconnected	GPIO Disconnected	**Port D 1**—When the DAX is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. This input is 5 V tolerant.

2.12 Timer

Table 2-14 Timer Signal

Signal Name	Type	State during Reset	Signal Description
TIO0	Input or Output	Input	**Timer 0 Schmitt-Trigger Input/Output**—When timer 0 functions as an external event counter or in measurement mode, TIO0 is used as input. When timer 0 functions in watchdog, timer, or pulse modulation mode, TIO0 is used as output. The default mode after reset is GPIO input. This can be changed to output or configured as a timer input/output through the timer 0 control/status register (TCSR0). If TIO0 is not being used, it is recommended to either define it as GPIO output immediately at the beginning of operation or leave it defined as GPIO input but connected to Vcc through a pull-up resistor in order to ensure a stable logic level at this input. *This input is 5 V tolerant.*

2.13 JTAG/OnCE Interface

Table 2-15 JTAG/OnCE Interface

Signal Name	Signal Type	State during Reset	Signal Description
TCK	Input	Input	**Test Clock**—TCK is a test clock input signal used to synchronize the JTAG test logic. It has an internal pull-up resistor. *This input is 5 V tolerant.*
TDI	Input	Input	**Test Data Input**—TDI is a test data serial input signal used for test instructions and data. TDI is sampled on the rising edge of TCK and has an internal pull-up resistor. This input is 5 V tolerant.
TDO	Output	Tri-stated	**Test Data Output**—TDO is a test data serial output signal used for test instructions and data. TDO is tri-statable and is actively driven in the shift-IR and shift-DR controller states. TDO changes on the falling edge of TCK.
TMS	Input	Input	**Test Mode Select**—TMS is an input signal used to sequence the test controller's state machine. TMS is sampled on the rising edge of TCK and has an internal pull-up resistor. This input is 5 V tolerant.

NOTES

3 Specifications

3.1 Introduction

The DSP56366 is a high density CMOS device with Transistor-Transistor Logic (TTL) compatible inputs and outputs. The DSP56366 specifications are preliminary and are from design simulations, and may not be fully tested or guaranteed. Finalized specifications will be published after full characterization and device qualifications are complete.

3.2 Maximum Ratings

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields. However, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability of operation is enhanced if unused inputs are pulled to an appropriate logic voltage level (e.g., either GND or V_{CC}). The suggested value for a pullup or pulldown resistor is 10 kΩ.

NOTE

In the calculation of timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a "maximum" value for a specification will never occur in the same device that has a "minimum" value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 3-1 Maximum Ratings

Rating[1]	Symbol	Value[1, 2]	Unit
Supply Voltage	V_{CC}	−0.3 to +4.0	V
All input voltages excluding "5 V tolerant" inputs[3]	V_{IN}	GND -0.3 to V_{CC} + 0.3	V
All "5 V tolerant" input voltages[3]	V_{IN5}	GND − 0.3 to V_{CC} + 3.95	V
Current drain per pin excluding V_{CC} and GND	I	10	mA

Table 3-1 Maximum Ratings (continued)

Rating[1]	Symbol	Value[1, 2]	Unit
Operating temperature range	T_J	−40 to +110	°C
Storage temperature	T_{STG}	−55 to +125	°C

1 GND = 0 V, V_{CC} = 3.3 V ± 0.16 V, T_J = –40°C to +110°C, C_L = 50 pF

2 Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the maximum rating may affect device reliability or cause permanent damage to the device.

3 **CAUTION:** All “5 V Tolerant” input voltages must not be more than 3.95 V greater than the supply voltage; this restriction applies to “power on”, as well as during normal operation. In any case, the input voltages cannot be more than 5.75 V. “5 V Tolerant” inputs are inputs that tolerate 5 V.

3.3 Thermal Characteristics

Table 3-2 Thermal Characteristics

Characteristic	Symbol	LQFP Value	Unit
Junction-to-ambient thermal resistance[1, 2] Natural Convection	$R_{\theta JA}$ or θ_{JA}	37	°C/W
Junction-to-case thermal resistance[3]	$R_{\theta JC}$ or θ_{JC}	7	°C/W
Thermal characterization parameter[4] Natural Convection	Ψ_{JT}	2.0	°C/W

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.

3 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

4 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

3.4 DC Electrical Characteristics

Table 3-3 DC Electrical Characteristics[1]

Characteristics	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	3.14	3.3	3.46	V
Input high voltage					V
• D(0:23), $\overline{BG}$, $\overline{BB}$, $\overline{TA}$, ESAI_1$_{(except\ SDO4_1)}$	V_{IH}	2.0	—		
• MOD[2]/$\overline{IRQ}$[2], $\overline{RESET}$, PINIT/$\overline{NMI}$ and all JTAG/ESAI/Timer/HDI08/DAX/ESAI_1$_{(only\ SDO4_1)}$/SHI$_{(SPI\ mode)}$	V_{IHP}	2.0	—	V_{CC} + 3.95	
• SHI$_{(I2C\ mode)}$	V_{IHP}	1.5	—	V_{CC} + 3.95	
• EXTAL[3]	V_{IHX}	0.8 × V_{CC}	—	V_{CC}	
Input low voltage					V
• D(0:23), $\overline{BG}$, $\overline{BB}$, $\overline{TA}$, ESAI_1$_{(except\ SDO4_1)}$	V_{IL}	–0.3	—	0.8	
• MOD[2]/$\overline{IRQ}$[2], $\overline{RESET}$, PINIT/$\overline{NMI}$ and all JTAG/ESAI/Timer/HDI08/DAX/ESAI_1$_{(only\ SDO4_1)}$/SHI$_{(SPI\ mode)}$	V_{ILP}	–0.3	—	0.8	
• SHI$_{(I2C\ mode)}$	V_{ILP}	–0.3	—	0.3 x V_{CC}	
• EXTAL[3]	V_{ILX}	–0.3	—	0.2 x V_{CC}	
Input leakage current	I_{IN}	–10	—	10	μA
High impedance (off-state) input current (@ 2.4 V / 0.4 V)	I_{TSI}	–10	—	10	μA
Output high voltage					V
• TTL (I_{OH} = –0.4 mA)[4,5]	V_{OH}	2.4	—	—	
• CMOS (I_{OH} = –10 μA)[4]	V_{OH}	V_{CC} – 0.01	—	—	
Output low voltage					V
• TTL (I_{OL} = 3.0 mA, open-drain pins I_{OL} = 6.7 mA)[4,5]	V_{OL}	—	—	0.4	
• CMOS (I_{OL} = 10 μA)[4]	V_{OL}	—	—	0.01	
Internal supply current[6] at internal clock of 120MHz					mA
• In Normal mode	I_{CCI}	—	116	200	
• In Wait mode	I_{CCW}	—	7.3	25	
• In Stop mode[7]	I_{CCS}	—	1	10	
PLL supply current		—	1	2.5	mA
Input capacitance[4]	C_{IN}	—	—	10	pF

1 V_{CC} = 3.3 V ± .16 V; T_J = – 40°C to +110°C, C_L = 50 pF

2 Refers to MODA/$\overline{IRQA}$, MODB/$\overline{IRQB}$, MODC/$\overline{IRQC}$,and MODD/$\overline{IRQD}$ pins.

3 Driving EXTAL to the low V_{IHX} or the high V_{ILX} value may cause additional power consumption (DC current). To minimize power consumption, the minimum V_{IHX} should be no lower than 0.9 × V_{CC} and the maximum V_{ILX} should be no higher than 0.1 × V_{CC}.

4 Periodically sampled and not 100% tested.

5 This characteristic does not apply to PCAP.

[6] Appendix A, "Power Consumption Benchmark" provides a formula to compute the estimated current requirements in Normal mode. In order to obtain these results, all inputs must be terminated (i.e., not allowed to float). Measurements are based on synthetic intensive DSP benchmarks. The power consumption numbers in this specification are 90% of the measured results of this benchmark. This reflects typical DSP applications. Typical internal supply current is measured with V_{CC} = 3.3 V at T_J = 110°C. Maximum internal supply current is measured with V_{CC} = 3.46 V at T_J = 110°C.

[7] In order to obtain these results, all inputs, which are not disconnected at Stop mode, must be terminated (i.e., not allowed to float).

3.5 AC Electrical Characteristics

The timing waveforms shown in the AC electrical characteristics section are tested with a V_{IL} maximum of 0.3 V and a V_{IH} minimum of 2.4 V for all pins except EXTAL, which is tested using the input levels shown in Note 3 of the previous table. AC timing specifications, which are referenced to a device input signal, are measured in production with respect to the 50% point of the respective input signal's transition. DSP56366 output levels are measured with the production test machine V_{OL} and V_{OH} reference levels set at 0.4 V and 2.4 V, respectively.

NOTE

Although the minimum value for the frequency of EXTAL is 0 MHz, the device AC test conditions are 15 MHz and rated speed.

3.6 Internal Clocks

Table 3-4 Internal Clocks

Characteristics	Symbol	Expression[1, 2]		
		Min	Typ	Max
Internal operation frequency with PLL enabled	f	—	(Ef × MF)/(PDF × DF)	—
Internal operation frequency with PLL disabled	f	—	Ef/2	—
Internal clock high period	T_H			
• With PLL disabled		—	ET_C	—
• With PLL enabled and MF ≤ 4		0.49 × ET_C × PDF × DF/MF	—	0.51 × ET_C × PDF × DF/MF
• With PLL enabled and MF > 4		0.47 × ET_C × PDF × DF/MF	—	0.53 × ET_C × PDF × DF/MF
Internal clock low period	T_L			
• With PLL disabled		—	ET_C	—
• With PLL enabled and MF ≤ 4		0.49 × ET_C × PDF × DF/MF	—	0.51 × ET_C × PDF × DF/MF
• With PLL enabled and MF > 4		0.47 × ET_C × PDF × DF/MF	—	0.53 × ET_C × PDF × DF/MF
Internal clock cycle time with PLL enabled	T_C	—	ET_C × PDF × DF/MF	—

Table 3-4 Internal Clocks

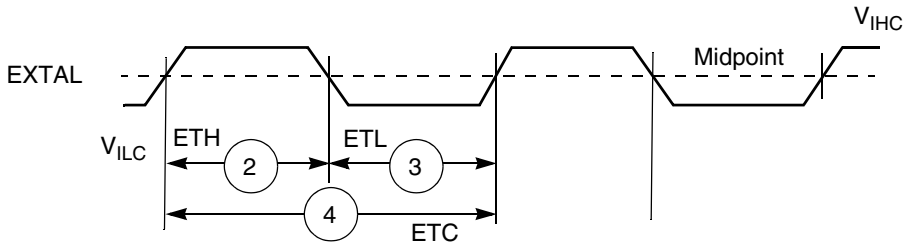
Characteristics	Symbol	Expression[1, 2]		
		Min	Typ	Max
Internal clock cycle time with PLL disabled	T_C	—	2 × ET_C	—
Instruction cycle time	I_{CYC}	—	T_C	—

1 DF = Division Factor
Ef = External frequency
ET_C = External clock cycle
MF = Multiplication Factor
PDF = Predivision Factor
T_C = internal clock cycle

2 See the **PLL and Clock Generation** section in the *DSP56300 Family Manual* for a detailed discussion of the PLL.

3.7 EXTERNAL CLOCK OPERATION

The DSP56366 system clock is an externally supplied square wave voltage source connected to EXTAL (See Figure 3-1).



Notes The midpoint is 0.5 (V_{IHC} + V_{ILC}).

Figure 3-1 External Clock Timing

Table 3-5 Clock Operation

No.	Characteristics	Symbol	Min	Max
1	Frequency of EXTAL (EXTAL Pin Frequency) The rise and fall time of this external clock should be 3 ns maximum.	Ef	0	120.0
2	EXTAL input high[1, 2] • With PLL disabled (46.7%–53.3% duty cycle[3]) • With PLL enabled (42.5%–57.5% duty cycle[3])	ET_H	 3.89 ns 3.54 ns	 ∞ 157.0 µs
3	EXTAL input low[1, 2] • With PLL disabled (46.7%–53.3% duty cycle[3]) • With PLL enabled (42.5%–57.5% duty cycle[3])	ET_L	 3.89 ns 3.54 ns	 ∞ 157.0 µs

Table 3-5 Clock Operation (continued)

No.	Characteristics	Symbol	Min	Max
4	EXTAL cycle time[2] • With PLL disabled • With PLL enabled	ET_C	 8.33 ns 8.33 ns	 ∞ 273.1 µs
7	Instruction cycle time = $I_{CYC} = T_C$[4, 2] • With PLL disabled • With PLL enabled	I_{CYC}	 16.66 ns 8.33 ns	 ∞ 8.53 µs

1 Measured at 50% of the input transition.
2 The maximum value for PLL enabled is given for minimum V_{CO} and maximum MF.
3 The indicated duty cycle is for the specified maximum frequency for which a part is rated. The minimum clock high or low time required for correct operation, however, remains the same at lower operating frequencies; therefore, when a lower clock frequency is used, the signal symmetry may vary from the specified duty cycle as long as the minimum high time and low time requirements are met.
4 The maximum value for PLL enabled is given for minimum VCO and maximum DF.

3.8 Phase Lock Loop (PLL) Characteristics

Table 3-6 PLL Characteristics

Characteristics	Min	Max	Unit
V_{CO} frequency when PLL enabled (MF × E_f × 2/PDF)	30	240	MHz
PLL external capacitor (PCAP pin to V_{CCP}) (C_{PCAP})[1] • @ MF ≤ 4 • @ MF > 4	 (MF × 580) – 100 MF × 830	 (MF × 780) – 140 MF × 1470	pF

1 C_{PCAP} is the value of the PLL capacitor (connected between the PCAP pin and V_{CCP}). The recommended value in pF for C_{PCAP} can be computed from one of the following equations:
(MF x 680)-120, for MF ≤ 4 or MF x 1100, for MF > 4.

3.9 Reset, Stop, Mode Select, and Interrupt Timing

Table 3-7 Reset, Stop, Mode Select, and Interrupt Timing[1]

No.	Characteristics	Expression	Min	Max	Unit
8	Delay from $\overline{\text{RESET}}$ assertion to all pins at reset value[2]	—	—	26.0	ns
9	Required $\overline{\text{RESET}}$ duration[3]				
	• Power on, external clock generator, PLL disabled	50 × ET_C	416.7	—	ns
	• Power on, external clock generator, PLL enabled	1000 × ET_C	8.3	—	µs
	• During normal operation	2.5 × T_C	20.8	—	ns
10	Delay from asynchronous $\overline{\text{RESET}}$ deassertion to first external address output (internal reset deassertion)[4]				
	• Minimum	3.25 × T_C + 2.0	29.1	—	ns
	• Maximum	20.25 T_C + 7.50	—	176.2	ns
13	Mode select setup time		30.0	—	ns

Table 3-7 Reset, Stop, Mode Select, and Interrupt Timing[1] (continued)

No.	Characteristics	Expression	Min	Max	Unit
14	Mode select hold time		0.0	—	ns
15	Minimum edge-triggered interrupt request assertion width		5.5	—	ns
16	Minimum edge-triggered interrupt request deassertion width		5.5	—	ns
17	Delay from $\overline{IRQA}$, $\overline{IRQB}$, $\overline{IRQC}$, $\overline{IRQD}$, $\overline{NMI}$ assertion to external memory access address out valid				
	• Caused by first interrupt instruction fetch	$4.25 \times T_C + 2.0$	37.4	—	ns
	• Caused by first interrupt instruction execution	$7.25 \times T_C + 2.0$	62.4	—	ns
18	Delay from $\overline{IRQA}$, $\overline{IRQB}$, $\overline{IRQC}$, $\overline{IRQD}$, $\overline{NMI}$ assertion to general-purpose transfer output valid caused by first interrupt instruction execution	$10 \times T_C + 5.0$	88.3	—	ns
19	Delay from address output valid caused by first interrupt instruction execute to interrupt request deassertion for level sensitive fast interrupts[5]	$3.75 \times T_C + WS \times T_C - 10.94$	—	Note[6]	ns
20	Delay from $\overline{RD}$ assertion to interrupt request deassertion for level sensitive fast interrupts[5]	$3.25 \times T_C + WS \times T_C - 10.94$	—	Note 6	ns
21	Delay from $\overline{WR}$ assertion to interrupt request deassertion for level sensitive fast interrupts[5]				ns
	• DRAM for all WS	$(WS + 3.5) \times T_C - 10.94$	—	Note 6	
	• SRAM WS = 1	$(WS + 3.5) \times T_C - 10.94$	—	Note 6	
	• SRAM WS = 2, 3	$(WS + 3) \times T_C - 10.94$	—	Note 6	
	• SRAM WS $\geq$ 4	$(WS + 2.5) \times T_C - 10.94$	—	Note 6	
24	Duration for $\overline{IRQA}$ assertion to recover from Stop state		4.9	—	
25	Delay from $\overline{IRQA}$ assertion to fetch of first instruction (when exiting Stop)[2, 7]				
	• PLL is not active during Stop (PCTL Bit 17 = 0) and Stop delay is enabled (OMR Bit 6 = 0)	$PLC \times ET_C \times PDF + (128\ K - PLC/2) \times T_C$	—	—	ms
	• PLL is not active during Stop (PCTL Bit 17 = 0) and Stop delay is not enabled (OMR Bit 6 = 1)	$PLC \times ET_C \times PDF + (23.75 \pm 0.5) \times T_C$	—	—	ms
	• PLL is active during Stop (PCTL Bit 17 = 1) (Implies No Stop Delay)	$(8.25 \pm 0.5) \times T_C$	64.6	72.9	ms
26	Duration of level sensitive $\overline{IRQA}$ assertion to ensure interrupt service (when exiting Stop)[2, 7]				
	• PLL is not active during Stop (PCTL Bit 17 = 0) and Stop delay is enabled (OMR Bit 6 = 0)	$PLC \times ET_C \times PDF + (128K - PLC/2) \times T_C$	—	—	ms
	• PLL is not active during Stop (PCTL Bit 17 = 0) and Stop delay is not enabled (OMR Bit 6 = 1)	$PLC \times ET_C \times PDF + (20.5 \pm 0.5) \times T_C$	—	—	ms
	• PLL is active during Stop (PCTL Bit 17 = 1) (implies no Stop delay)	$5.5 \times T_C$	45.8	—	ns

Table 3-7 Reset, Stop, Mode Select, and Interrupt Timing[1] (continued)

No.	Characteristics	Expression	Min	Max	Unit
27	Interrupt Requests Rate				
	• HDI08, ESAI, ESAI_1, SHI, DAX, Timer	$12T_C$	—	100.0	ns
	• DMA	$8T_C$	—	66.7	ns
	• $\overline{\text{IRQ}}$, $\overline{\text{NMI}}$ (edge trigger)	$8T_C$	—	66.7	ns
	• $\overline{\text{IRQ}}$ (level trigger)	$12T_C$	—	100.0	ns
28	DMA Requests Rate				
	• Data read from HDI08, ESAI, ESAI_1, SHI, DAX	$6T_C$	—	50.0	ns
	• Data write to HDI08, ESAI, ESAI_1, SHI, DAX	$7T_C$	—	58.0	ns
	• Timer	$2T_C$		16.7	
	• $\overline{\text{IRQ}}$, $\overline{\text{NMI}}$ (edge trigger)	$3T_C$	—	25.0	ns
29	Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, $\overline{\text{NMI}}$ assertion to external memory (DMA source) access address out valid	$4.25 \times T_C + 2.0$	37.4	—	ns

1 V_{CC} = 3.3 V ± 0.16 V; T_J = –40°C to + 110°C, C_L = 50 pF

2 Periodically sampled and not 100% tested.

3 $\overline{\text{RESET}}$ duration is measured during the time in which $\overline{\text{RESET}}$ is asserted, V_{CC} is valid, and the EXTAL input is active and valid. When the V_{CC} is valid, but the other "required $\overline{\text{RESET}}$ duration" conditions (as specified above) have not been yet met, the device circuitry will be in an uninitialized state that can result in significant power consumption and heat-up. Designs should minimize this state to the shortest possible duration.

4 If PLL does not lose lock.

5 When using fast interrupts and $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, and $\overline{\text{IRQD}}$ are defined as level-sensitive, timings 19 through 21 apply to prevent multiple interrupt service. To avoid these timing restrictions, the deasserted Edge-triggered mode is recommended when using fast interrupts. Long interrupts are recommended when using Level-sensitive mode.

6 WS = number of wait states (measured in clock cycles, number of T_C). Use expression to compute maximum value.

7 This timing depends on several settings:

For PLL disable, using external clock (PCTL Bit 16 = 1), no stabilization delay is required and recovery time will be defined by the PCTL Bit 17 and OMR Bit 6 settings.

For PLL enable, if PCTL Bit 17 is 0, the PLL is shutdown during Stop. Recovering from Stop requires the PLL to get locked. The PLL lock procedure duration, PLL Lock Cycles (PLC), may be in the range of 0 to 1000 cycles. This procedure occurs in parallel with the stop delay counter, and stop recovery will end when the last of these two events occurs: the stop delay counter completes count or PLL lock procedure completion.

PLC value for PLL disable is 0.

The maximum value for ET_C is 4096 (maximum MF) divided by the desired internal frequency (i.e., for 120 MHz it is 4096/120 MHz = 34.1 μs). During the stabilization period, T_C, T_H, and T_L will not be constant, and their width may vary, so timing may vary as well.

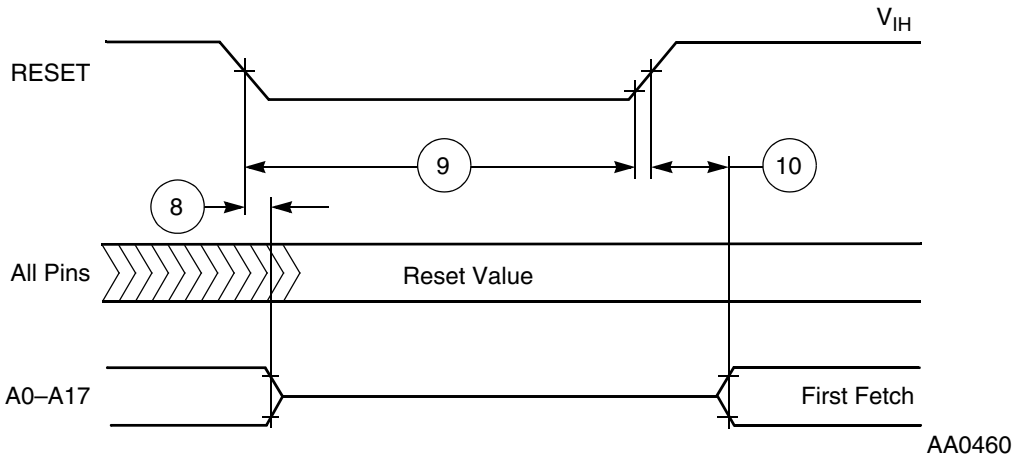


Figure 3-2 Reset Timing

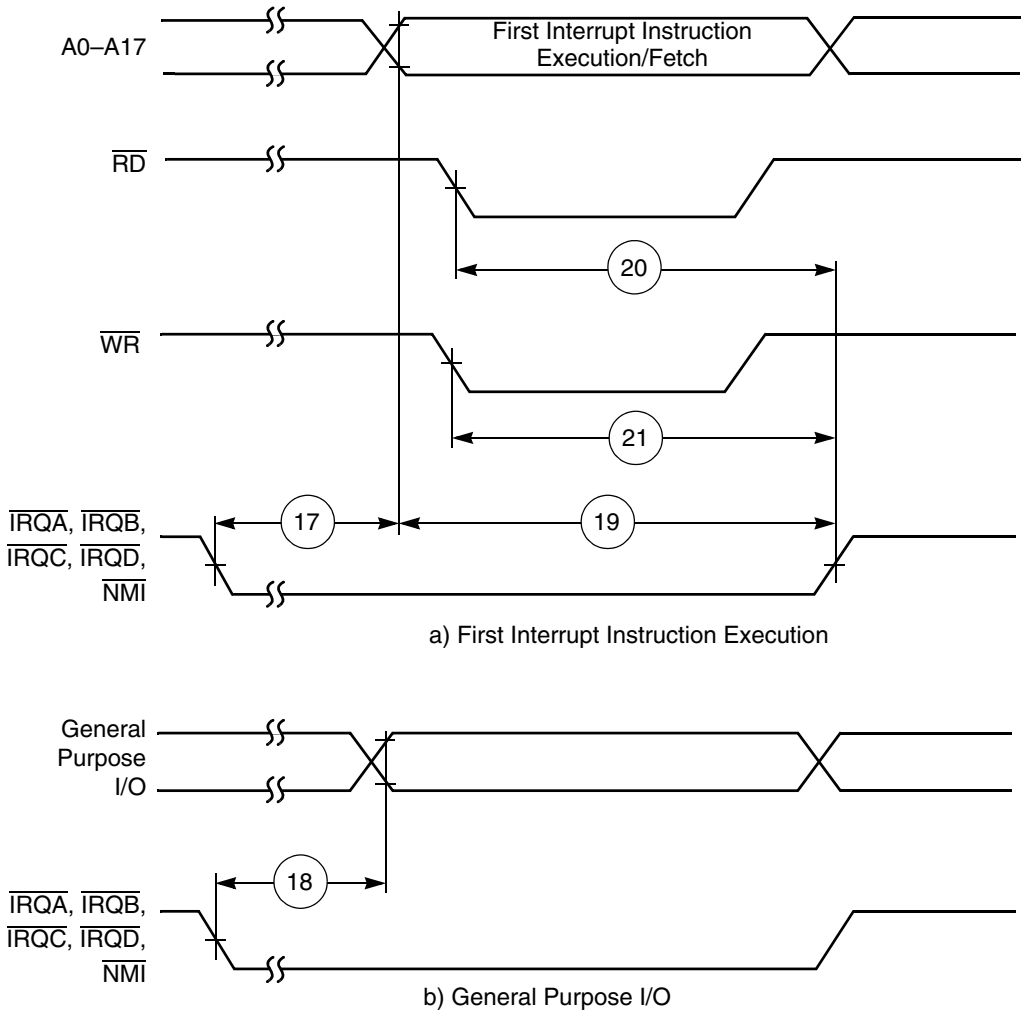


Figure 3-3 External Fast Interrupt Timing

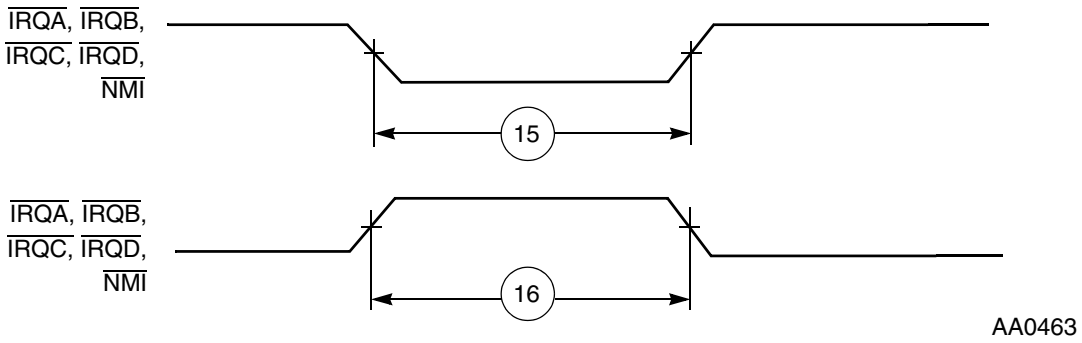


Figure 3-4 External Interrupt Timing (Negative Edge-Triggered)

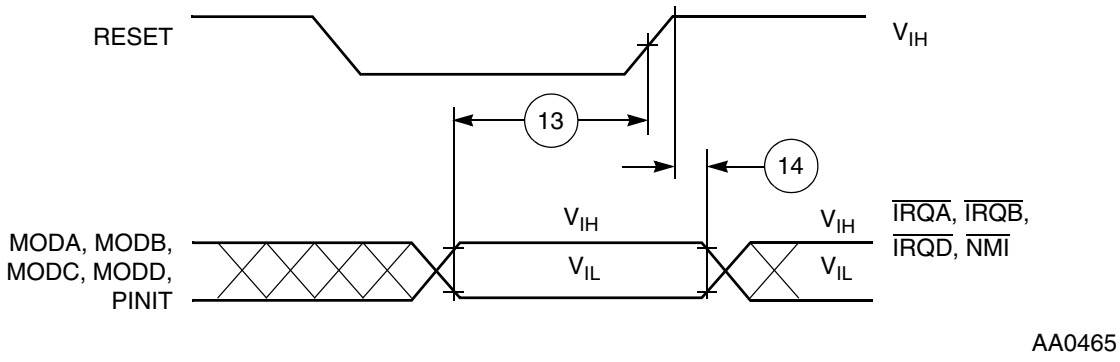


Figure 3-5 Operating Mode Select Timing

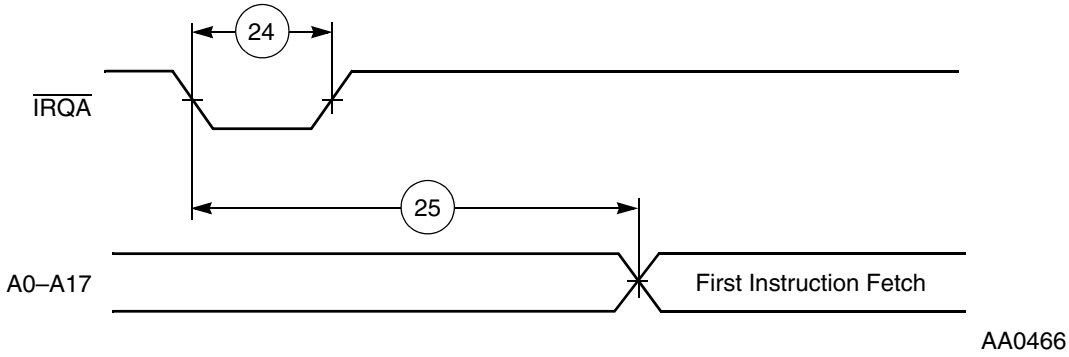


Figure 3-6 Recovery from Stop State Using IRQA

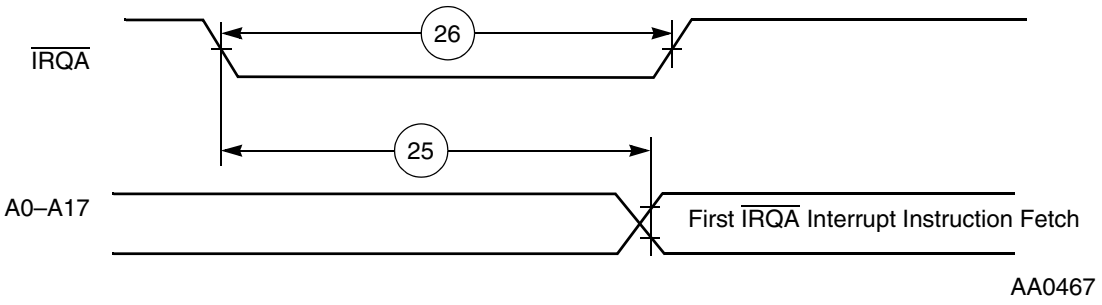


Figure 3-7 Recovery from Stop State Using IRQA Interrupt Service

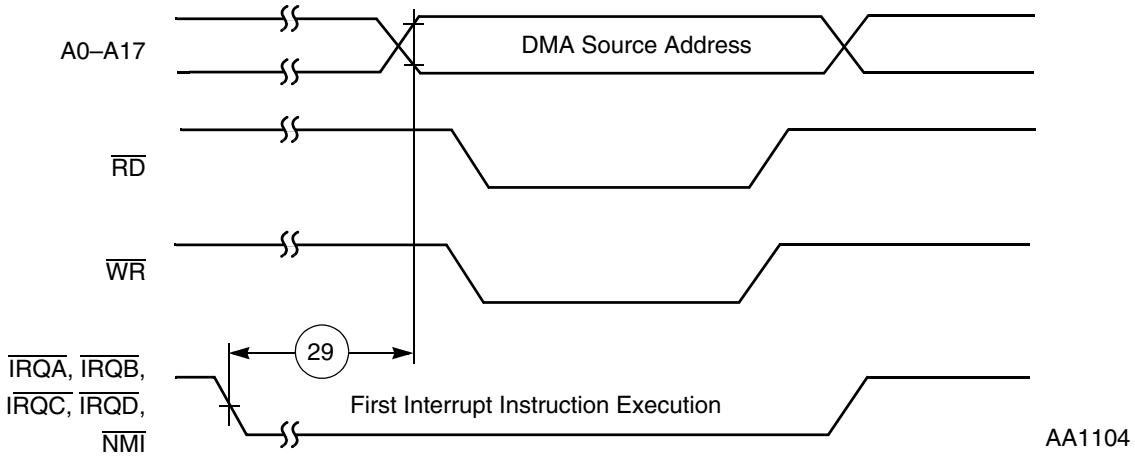


Figure 3-8 External Memory Access (DMA Source) Timing

3.10 External Memory Expansion Port (Port A)

3.10.1 SRAM Timing

Table 3-8 SRAM Read and Write Accesses[1]

No.	Characteristics	Symbol	Expression[2]	Min	Max	Unit
100	Address valid and AA assertion pulse width	t_{RC}, t_{WC}	$(WS + 1) \times T_C - 4.0$ $[1 \le WS \le 3]$	12.0	—	ns
			$(WS + 2) \times T_C - 4.0$ $[4 \le WS \le 7]$	46.0	—	ns
			$(WS + 3) \times T_C - 4.0$ $[WS \ge 8]$	87.0	—	ns

Table 3-8 SRAM Read and Write Accesses[1] (continued)

No.	Characteristics	Symbol	Expression[2]	Min	Max	Unit
101	Address and AA valid to $\overline{WR}$ assertion	t_{AS}	$0.25 \times T_C - 2.0$ [WS = 1]	0.1	—	ns
			$1.25 \times T_C - 2.0$ [WS ≥ 4]	8.4	—	ns
102	$\overline{WR}$ assertion pulse width	t_{WP}	$1.5 \times T_C - 4.0$ [WS = 1]	8.5	—	ns
			All frequencies: $WS \times T_C - 4.0$ [2 ≤ WS ≤ 3]	12.7	—	ns
			$(WS - 0.5) \times T_C - 4.0$ [WS ≥ 4]	25.2	—	ns
103	$\overline{WR}$ deassertion to address not valid	t_{WR}	$0.25 \times T_C - 2.0$ [1 ≤ WS ≤ 3]	0.1	—	ns
			$1.25 \times T_C - 2.0$ [4 ≤ WS ≤ 7]	8.4	—	ns
			$2.25 \times T_C - 2.0$ [WS ≥ 8]	16.7	—	ns
			All frequencies: $1.25 \times T_C - 4.0$ [4 ≤ WS ≤ 7]	6.4	—	ns
			$2.25 \times T_C - 4.0$ [WS ≥ 8]	14.7	—	ns
104	Address and AA valid to input data valid	t_{AA}, t_{AC}	$(WS + 0.75) \times T_C - 7.0$ [WS ≥ 1]	—	7.6	ns
105	$\overline{RD}$ assertion to input data valid	t_{OE}	$(WS + 0.25) \times T_C - 7.0$ [WS ≥ 1]	—	3.4	ns
106	$\overline{RD}$ deassertion to data not valid (data hold time)	t_{OHZ}		0.0	—	ns
107	Address valid to $\overline{WR}$ deassertion[3]	t_{AW}	$(WS + 0.75) \times T_C - 4.0$ [WS ≥ 1]	10.6	—	ns
108	Data valid to $\overline{WR}$ deassertion (data setup time)	t_{DS} (t_{DW})	$(WS - 0.25) \times T_C - 3.0$ [WS ≥ 1]	3.2	—	ns

Table 3-8 SRAM Read and Write Accesses[1] (continued)

No.	Characteristics	Symbol	Expression[2]	Min	Max	Unit
109	Data hold time from $\overline{WR}$ deassertion	t_{DH}	$0.25 \times T_C - 2.0$ [1 ≤ WS ≤ 3]	0.1	—	ns
			$1.25 \times T_C - 2.0$ [4 ≤ WS ≤ 7]	8.4	—	ns
			$2.25 \times T_C - 2.0$ [WS ≥ 8]	16.7	—	ns
110	$\overline{WR}$ assertion to data active	—	$0.75 \times T_C - 3.7$ [WS = 1]	2.5	—	ns
			$0.25 \times T_C - 3.7$ [2 ≤ WS ≤ 3]	0.0	—	
			$-0.25 \times T_C - 3.7$ [WS ≥ 4]	0.0	—	
111	$\overline{WR}$ deassertion to data high impedance	—	$0.25 \times T_C + 0.2$ [1 ≤ WS ≤ 3]	—	2.3	ns
			$1.25 \times T_C + 0.2$ [4 ≤ WS ≤ 7]	—	10.6	
			$2.25 \times T_C + 0.2$ [WS ≥ 8]	—	18.9	
112	Previous $\overline{RD}$ deassertion to data active (write)	—	$1.25 \times T_C - 4.0$ [1 ≤ WS ≤ 3]	6.4	—	ns
			$2.25 \times T_C - 4.0$ [4 ≤ WS ≤ 7]	14.7	—	
			$3.25 \times T_C - 4.0$ [WS ≥ 8]	23.1	—	
113	$\overline{RD}$ deassertion time		$0.75 \times T_C - 4.0$ [1 ≤ WS ≤ 3]	2.2	—	ns
			$1.75 \times T_C - 4.0$ [4 ≤ WS ≤ 7]	10.6	—	ns
			$2.75 \times T_C - 4.0$ [WS ≥ 8]	18.9	—	ns

Table 3-8 SRAM Read and Write Accesses[1] (continued)

No.	Characteristics	Symbol	Expression[2]	Min	Max	Unit
114	$\overline{WR}$ deassertion time		$0.5 \times T_C - 4.0$ [WS = 1]	0.2	—	ns
			$T_C - 2.0$ [2 ≤ WS ≤ 3]	6.3	—	ns
			$2.5 \times T_C - 4.0$ [4 ≤ WS ≤ 7]	16.8	—	ns
			$3.5 \times T_C - 4.0$ [WS ≥ 8]	25.2	—	ns
115	Address valid to $\overline{RD}$ assertion		$0.5 \times T_C - 4.0$	0.2	—	ns
116	$\overline{RD}$ assertion pulse width		$(WS + 0.25) \times T_C - 4.0$	6.4	—	ns
117	$\overline{RD}$ deassertion to address not valid		$0.25 \times T_C - 2.0$ [1 ≤ WS ≤ 3]	0.1	—	ns
			$1.25 \times T_C - 2.0$ [4 ≤ WS ≤ 7]	8.4	—	ns
			$2.25 \times T_C - 2.0$ [WS ≥ 8]	16.7	—	ns
118	$\overline{TA}$ setup before $\overline{RD}$ or $\overline{WR}$ deassertion[4]		$0.25 \times T_C + 2.0$	4.1	—	ns
119	$\overline{TA}$ hold after $\overline{RD}$ or $\overline{WR}$ deassertion			0.0	—	ns

1 All timings for 100 MHz are measured from 0.5 · Vcc to .05 · Vcc

2 WS is the number of wait states specified in the BCR.

3 Timings 100, 107 are guaranteed by design, not tested.

4 In the case of $\overline{TA}$ negation: timing 118 is relative to the deassertion edge of $\overline{RD}$ or WR were $\overline{TA}$ to remain active

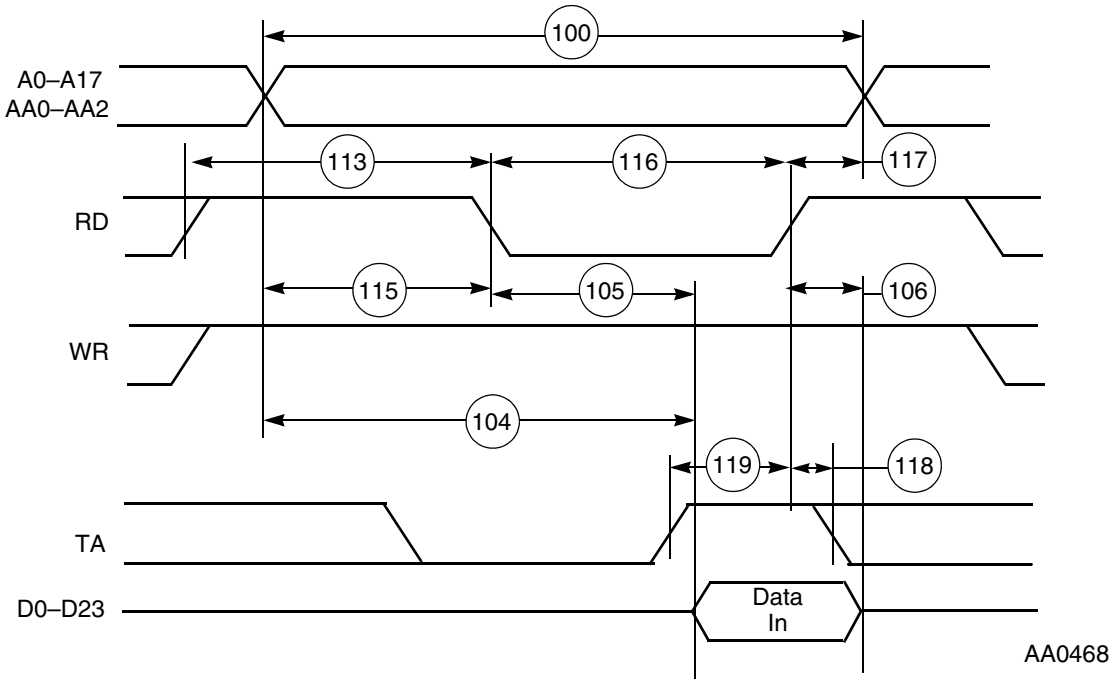


Figure 3-9 SRAM Read Access

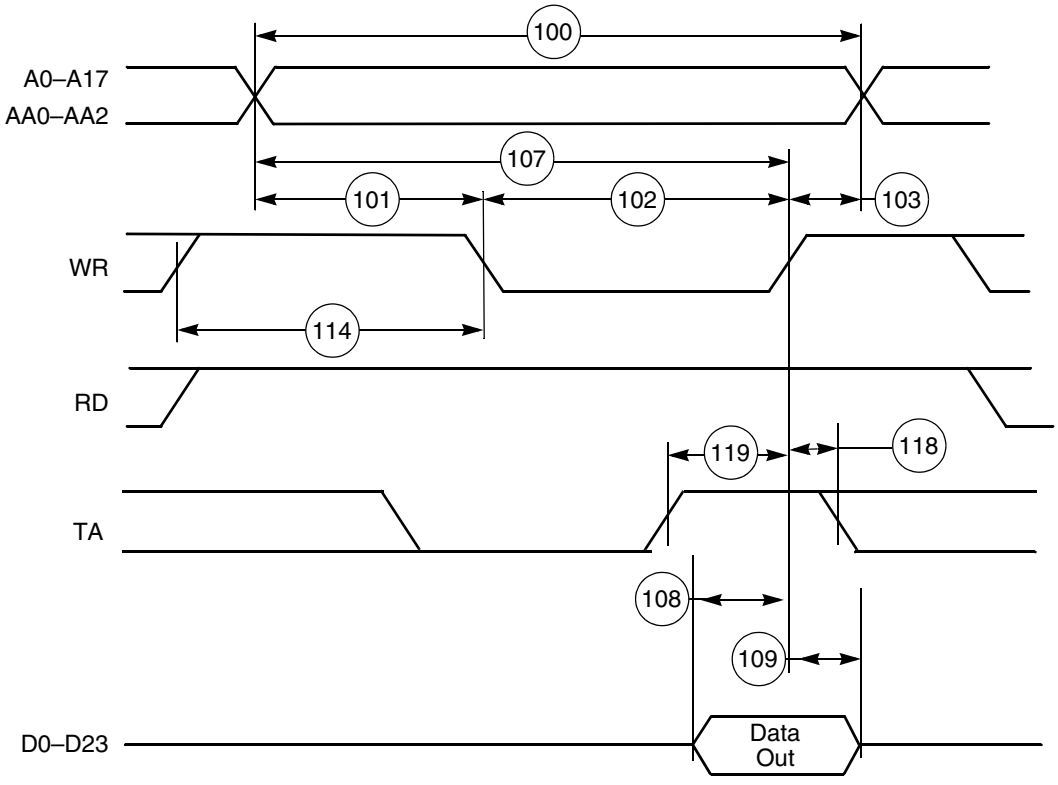


Figure 3-10 SRAM Write Access

3.10.2 DRAM Timing

The selection guides provided in Figure 3-11 and Figure 3-14 should be used for primary selection only. Final selection should be based on the timing provided in the following tables. As an example, the selection guide suggests that 4 wait states must be used for 100 MHz operation when using Page Mode DRAM. However, by using the information in the appropriate table, a designer may choose to evaluate whether fewer wait states might be used by determining which timing prevents operation at 100 MHz, running the chip at a slightly lower frequency (e.g., 95 MHz), using faster DRAM (if it becomes available), and control factors such as capacitive and resistive load to improve overall system performance.

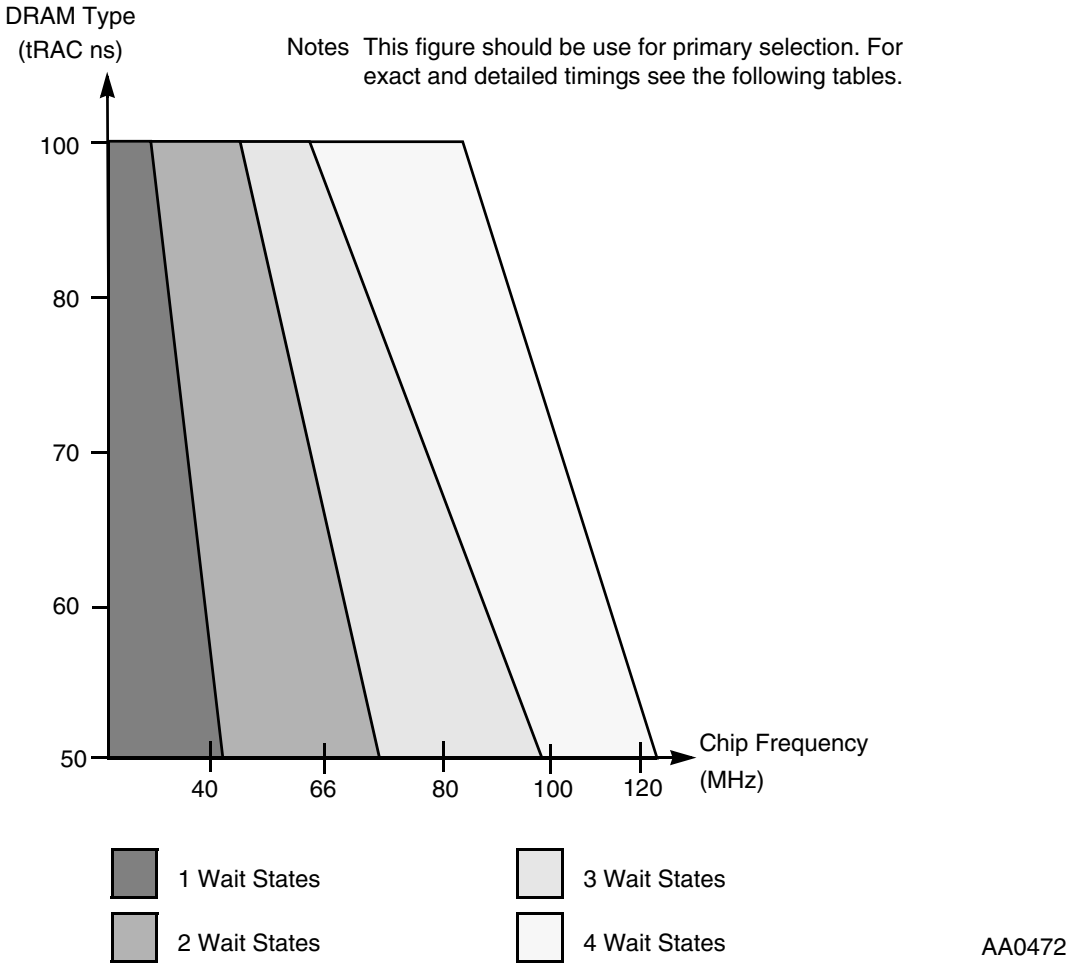


Figure 3-11 DRAM Page Mode Wait States Selection Guide

Table 3-9 DRAM Page Mode Timings, One Wait State (Low-Power Applications)[1, 2, 3]

No.	Characteristics	Symbol	Expression	20 MHz[4]		30 MHz[4]		Unit
				Min	Max	Min	Max	
131	Page mode cycle time for two consecutive accesses of the same direction Page mode cycle time for mixed (read and write) accesses	t_{PC}	$2 \times T_C$ $1.25 \times T_C$	100.0 62.5	— —	66.7 41.7	— —	ns
132	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	$T_C - 7.5$	—	42.5	—	25.8	ns
133	Column address valid to data valid (read)	t_{AA}	$1.5 \times T_C - 7.5$	—	67.5	—	42.5	ns
134	$\overline{CAS}$ deassertion to data not valid (read hold time)	t_{OFF}		0.0	—	0.0	—	ns
135	Last $\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$0.75 \times T_C - 4.0$	33.5	—	21.0	—	ns
136	Previous $\overline{CAS}$ deassertion to $\overline{RAS}$ deassertion	t_{RHCP}	$2 \times T_C - 4.0$	96.0	—	62.7	—	ns
137	$\overline{CAS}$ assertion pulse width	t_{CAS}	$0.75 \times T_C - 4.0$	33.5	—	21.0	—	ns
138	Last $\overline{CAS}$ deassertion to $\overline{RAS}$ deassertion[5] • BRW[1:0] = 00 • BRW[1:0] = 01 • BRW[1:0] = 10 • BRW[1:0] = 11	t_{CRP}	 $1.75 \times T_C - 6.0$ $3.25 \times T_C - 6.0$ $4.25 \times T_C - 6.0$ $6.25 \times T_C - 6.0$	 81.5 156.5 206.5 306.5	 — — — —	 52.3 102.2 135.5 202.1	 — — — —	ns
139	$\overline{CAS}$ deassertion pulse width	t_{CP}	$0.5 \times T_C - 4.0$	21.0	—	12.7	—	ns
140	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	$0.5 \times T_C - 4.0$	21.0	—	12.7	—	ns
141	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$0.75 \times T_C - 4.0$	33.5	—	21.0	—	ns
142	Last column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$2 \times T_C - 4.0$	96.0	—	62.7	—	ns
143	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$0.75 \times T_C - 3.8$	33.7	—	21.2	—	ns
144	$\overline{CAS}$ deassertion to $\overline{WR}$ assertion	t_{RCH}	$0.25 \times T_C - 3.7$	8.8	—	4.6	—	ns
145	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$0.5 \times T_C - 4.2$	20.8	—	12.5	—	ns
146	$\overline{WR}$ assertion pulse width	t_{WP}	$1.5 \times T_C - 4.5$	70.5	—	45.5	—	ns
147	Last $\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$1.75 \times T_C - 4.3$	83.2	—	54.0	—	ns
148	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	$1.75 \times T_C - 4.3$	83.2	—	54.0	—	ns
149	Data valid to $\overline{CAS}$ assertion (Write)	t_{DS}	$0.25 \times T_C - 4.0$	8.5	—	4.3	—	ns

Table 3-9 DRAM Page Mode Timings, One Wait State (Low-Power Applications)[1, 2, 3] (continued)

No.	Characteristics	Symbol	Expression	20 MHz[4]		30 MHz[4]		Unit
				Min	Max	Min	Max	
150	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$0.75 \times T_C - 4.0$	33.5	—	21.0	—	ns
151	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$T_C - 4.3$	45.7	—	29.0	—	ns
152	Last $\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$1.5 \times T_C - 4.0$	71.0	—	46.0	—	ns
153	$\overline{RD}$ assertion to data valid	t_{GA}	$T_C - 7.5$	—	42.5	—	25.8	ns
154	$\overline{RD}$ deassertion to data not valid[6]	t_{GZ}		0.0	—	0.0	—	ns
155	$\overline{WR}$ assertion to data active		$0.75 \times T_C - 0.3$	37.2	—	24.7	—	ns
156	$\overline{WR}$ deassertion to data high impedance		$0.25 \times T_C$	—	12.5	—	8.3	ns

1 The number of wait states for Page mode access is specified in the DCR.
2 The refresh period is specified in the DCR.
3 All the timings are calculated for the worst case. Some of the timings are better for specific cases (e.g., t_{PC} equals $2 \times T_C$ for read-after-read or write-after-write sequences).
4 Reduced DSP clock speed allows use of Page Mode DRAM with one Wait state (See Figure 3-14.).
5 BRW[1:0] (DRAM control register bits) defines the number of wait states that should be inserted in each DRAM out-of-page access.
6 $\overline{RD}$ deassertion will always occur after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.

Table 3-10 DRAM Page Mode Timings, Two Wait States[1, 2, 3, 4]

No.	Characteristics	Symbol	Expression[5]	66 MHz		80 MHz		Unit
				Min	Max	Min	Max	
131	Page mode cycle time for two consecutive accesses of the same direction	t_{PC}	$2 \times T_C$	45.4	—	37.5	—	ns
	Page mode cycle time for mixed (read and write) accesses		$1.25 \times T_C$	41.1	—	34.4	—	
132	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	$1.5 \times T_C - 7.5$	—	15.2	—	—	ns
			$1.5 \times T_C - 6.5$	—	—	—	12.3	ns
133	Column address valid to data valid (read)	t_{AA}	$2.5 \times T_C - 7.5$	—	30.4	—	—	ns
			$2.5 \times T_C - 6.5$	—	—	—	24.8	ns
134	$\overline{CAS}$ deassertion to data not valid (read hold time)	t_{OFF}		0.0	—	0.0	—	ns
135	Last $\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$1.75 \times T_C - 4.0$	22.5	—	17.9	—	ns
136	Previous $\overline{CAS}$ deassertion to $\overline{RAS}$ deassertion	t_{RHCP}	$3.25 \times T_C - 4.0$	45.2	—	36.6	—	ns
137	$\overline{CAS}$ assertion pulse width	t_{CAS}	$1.5 \times T_C - 4.0$	18.7	—	14.8	—	ns

Table 3-10 DRAM Page Mode Timings, Two Wait States[1, 2, 3, 4] (continued)

No.	Characteristics	Symbol	Expression[5]	66 MHz		80 MHz		Unit
				Min	Max	Min	Max	
138	Last $\overline{CAS}$ deassertion to $\overline{RAS}$ deassertion[6]	t_{CRP}						ns
	• BRW[1:0] = 00		$2.0 \times T_C - 6.0$	24.4	—	19.0	—	
	• BRW[1:0] = 01		$3.5 \times T_C - 6.0$	47.2	—	37.8	—	
	• BRW[1:0] = 10		$4.5 \times T_C - 6.0$	62.4	—	50.3	—	
	• BRW[1:0] = 11		$6.5 \times T_C - 6.0$	92.8	—	75.3	—	
139	$\overline{CAS}$ deassertion pulse width	t_{CP}	$1.25 \times T_C - 4.0$	14.9	—	11.6	—	ns
140	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	$T_C - 4.0$	11.2	—	8.5	—	ns
141	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$1.75 \times T_C - 4.0$	22.5	—	17.9	—	ns
142	Last column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$3 \times T_C - 4.0$	41.5	—	33.5	—	ns
143	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$1.25 \times T_C - 3.8$	15.1	—	11.8	—	ns
144	$\overline{CAS}$ deassertion to $\overline{WR}$ assertion	t_{RCH}	$0.5 \times T_C - 3.7$	3.9	—	2.6	—	ns
145	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$1.5 \times T_C - 4.2$	18.5	—	14.6	—	ns
146	$\overline{WR}$ assertion pulse width	t_{WP}	$2.5 \times T_C - 4.5$	33.5	—	26.8	—	ns
147	Last $\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$2.75 \times T_C - 4.3$	33.4	—	26.8	—	ns
148	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	$2.5 \times T_C - 4.3$	33.6	—	27.0	—	ns
149	Data valid to $\overline{CAS}$ assertion (write)	t_{DS}	$0.25 \times T_C - 3.7$	0.1	—	—	—	ns
			$0.25 \times T_C - 3.0$	—	—	0.1	—	
150	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$1.75 \times T_C - 4.0$	22.5	—	17.9	—	ns
151	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$T_C - 4.3$	10.9	—	8.2	—	ns
152	Last $\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$2.5 \times T_C - 4.0$	33.9	—	27.3	—	ns
153	$\overline{RD}$ assertion to data valid	t_{GA}	$1.75 \times T_C - 7.5$	—	19.0	—	—	ns
			$1.75 \times T_C - 6.5$	—	—	—	15.4	
154	$\overline{RD}$ deassertion to data not valid[7]	t_{GZ}		0.0	—	0.0	—	ns
155	$\overline{WR}$ assertion to data active		$0.75 \times T_C - 0.3$	11.1	—	9.1	—	ns
156	$\overline{WR}$ deassertion to data high impedance		$0.25 \times T_C$	—	3.8	—	3.1	ns

1 The number of wait states for Page mode access is specified in the DCR.
2 The refresh period is specified in the DCR.
3 The asynchronous delays specified in the expressions are valid for DSP56366.
4 There are no DRAMs fast enough to fit to two wait states Page mode @ 100MHz (See Figure 3-11)

[5] All the timings are calculated for the worst case. Some of the timings are better for specific cases (e.g., t_{PC} equals $3 \times T_C$ for read-after-read or write-after-write sequences).

[6] BRW[1:0] (DRAM Control Register bits) defines the number of wait states that should be inserted in each DRAM out-of-page access.

[7] $\overline{RD}$ deassertion will always occur after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.

Table 3-11 DRAM Page Mode Timings, Three Wait States[1, 2, 3]

No.	Characteristics	Symbol	Expression[4]	Min	Max	Unit
131	Page mode cycle time for two consecutive accesses of the same direction	t_{PC}	$2 \times T_C$	40.0	—	ns
	Page mode cycle time for mixed (read and write) accesses		$1.25 \times T_C$	35.0	—	
132	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	$2 \times T_C - 7.0$	—	13.0	ns
133	Column address valid to data valid (read)	t_{AA}	$3 \times T_C - 7.0$	—	23.0	ns
134	$\overline{CAS}$ deassertion to data not valid (read hold time)	t_{OFF}		0.0	—	ns
135	Last $\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$2.5 \times T_C - 4.0$	21.0	—	ns
136	Previous $\overline{CAS}$ deassertion to $\overline{RAS}$ deassertion	t_{RHCP}	$4.5 \times T_C - 4.0$	41.0	—	ns
137	$\overline{CAS}$ assertion pulse width	t_{CAS}	$2 \times T_C - 4.0$	16.0	—	ns
138	Last $\overline{CAS}$ deassertion to $\overline{RAS}$ assertion[5]	t_{CRP}				ns
	• BRW[1:0] = 00		$2.25 \times T_C - 6.0$	—	—	
	• BRW[1:0] = 01		$3.75 \times T_C - 6.0$	—	—	
	• BRW[1:0] = 10		$4.75 \times T_C - 6.0$	41.5	—	
	• BRW[1:0] = 11		$6.75 \times T_C - 6.0$	61.5	—	
139	$\overline{CAS}$ deassertion pulse width	t_{CP}	$1.5 \times T_C - 4.0$	11.0	—	ns
140	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	$T_C - 4.0$	6.0	—	ns
141	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$2.5 \times T_C - 4.0$	21.0	—	ns
142	Last column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$4 \times T_C - 4.0$	36.0	—	ns
143	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$1.25 \times T_C - 4.0$	8.5	—	ns
144	$\overline{CAS}$ deassertion to $\overline{WR}$ assertion	t_{RCH}	$0.75 \times T_C - 4.0$	3.5	—	ns
145	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$2.25 \times T_C - 4.2$	18.3	—	ns
146	$\overline{WR}$ assertion pulse width	t_{WP}	$3.5 \times T_C - 4.5$	30.5	—	ns
147	Last $\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$3.75 \times T_C - 4.3$	33.2	—	ns
148	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	$3.25 \times T_C - 4.3$	28.2	—	ns
149	Data valid to $\overline{CAS}$ assertion (write)	t_{DS}	$0.5 \times T_C - 4.0$	1.0	—	ns

Table 3-11 DRAM Page Mode Timings, Three Wait States[1, 2, 3] (continued)

No.	Characteristics	Symbol	Expression[4]	Min	Max	Unit
150	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$2.5 \times T_C - 4.0$	21.0	—	ns
151	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$1.25 \times T_C - 4.3$	8.2	—	ns
152	Last $\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$3.5 \times T_C - 4.0$	31.0	—	ns
153	$\overline{RD}$ assertion to data valid	t_{GA}	$2.5 \times T_C - 7.0$	—	18.0	ns
154	$\overline{RD}$ deassertion to data not valid[6]	t_{GZ}		0.0	—	ns
155	$\overline{WR}$ assertion to data active		$0.75 \times T_C - 0.3$	7.2	—	ns
156	$\overline{WR}$ deassertion to data high impedance		$0.25 \times T_C$	—	2.5	ns

1 The number of wait states for Page mode access is specified in the DCR.
2 The refresh period is specified in the DCR.
3 The asynchronous delays specified in the expressions are valid for DSP56366.
4 All the timings are calculated for the worst case. Some of the timings are better for specific cases (e.g., t_{PC} equals $4 \times T_C$ for read-after-read or write-after-write sequences).
5 BRW[1:0] (DRAM control register bits) defines the number of wait states that should be inserted in each DRAM out-of page-access.
6 $\overline{RD}$ deassertion will always occur after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.

Table 3-12 DRAM Page Mode Timings, Four Wait States[1, 2, 3]

No.	Characteristics	Symbol	Expression[4]	Min	Max	Unit
131	Page mode cycle time for two consecutive accesses of the same direction. Page mode cycle time for mixed (read and write) accesses	t_{PC}	$5 \times T_C$ $4.5 \times T_C$	41.7 37.5	— —	ns
132	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	$2.75 \times T_C - 7.0$	—	15.9	ns
133	Column address valid to data valid (read)	t_{AA}	$3.75 \times T_C - 7.0$	—	24.2	ns
134	$\overline{CAS}$ deassertion to data not valid (read hold time)	t_{OFF}		0.0	—	ns
135	Last $\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$3.5 \times T_C - 4.0$	25.2	—	ns
136	Previous $\overline{CAS}$ deassertion to $\overline{RAS}$ deassertion	t_{RHCP}	$6 \times T_C - 4.0$	46.0	—	ns
137	$\overline{CAS}$ assertion pulse width	t_{CAS}	$2.5 \times T_C - 4.0$	16.8	—	ns
138	Last $\overline{CAS}$ deassertion to $\overline{RAS}$ assertion[5] • BRW[1:0] = 00 • BRW[1:0] = 01 • BRW[1:0] = 10 • BRW[1:0] = 11	t_{CRP}	 $2.75 \times T_C - 6.0$ $4.25 \times T_C - 6.0$ $5.25 \times T_C - 6.0$ $7.25 \times T_C - 6.0$	 — — 37.7 54.4	 — — — —	ns
139	$\overline{CAS}$ deassertion pulse width	t_{CP}	$2 \times T_C - 4.0$	12.7	—	ns

Table 3-12 DRAM Page Mode Timings, Four Wait States[1, 2, 3] (continued)

No.	Characteristics	Symbol	Expression[4]	Min	Max	Unit
140	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	$T_C - 4.0$	4.3	—	ns
141	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$3.5 \times T_C - 4.0$	25.2	—	ns
142	Last column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$5 \times T_C - 4.0$	37.7	—	ns
143	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$1.25 \times T_C - 4.0$	6.4	—	ns
144	$\overline{CAS}$ deassertion to $\overline{WR}$ assertion	t_{RCH}	$1.25 \times T_C - 4.0$	6.4	—	ns
145	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$3.25 \times T_C - 4.2$	22.9	—	ns
146	$\overline{WR}$ assertion pulse width	t_{WP}	$4.5 \times T_C - 4.5$	33.0	—	ns
147	Last $\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$4.75 \times T_C - 4.3$	35.3	—	ns
148	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	$3.75 \times T_C - 4.3$	26.9	—	ns
149	Data valid to $\overline{CAS}$ assertion (write)	t_{DS}	$0.5 \times T_C - 4.0$	0.2	—	ns
150	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$3.5 \times T_C - 4.0$	25.2	—	ns
151	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$1.25 \times T_C - 4.3$	6.1	—	ns
152	Last $\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$4.5 \times T_C - 4.0$	33.5	—	ns
153	$\overline{RD}$ assertion to data valid	t_{GA}	$3.25 \times T_C - 7.0$	—	20.1	ns
154	$\overline{RD}$ deassertion to data not valid[6]	t_{GZ}		0.0	—	ns
155	$\overline{WR}$ assertion to data active		$0.75 \times T_C - 0.3$	5.9	—	ns
156	$\overline{WR}$ deassertion to data high impedance		$0.25 \times T_C$	—	2.1	ns

1 The number of wait states for Page mode access is specified in the DCR.

2 The refresh period is specified in the DCR.

3 The asynchronous delays specified in the expressions are valid for DSP56366.

4 All the timings are calculated for the worst case. Some of the timings are better for specific cases (e.g., t_{PC} equals $3 \times T_C$ for read-after-read or write-after-write sequences).

5 BRW[1:0] (DRAM control register bits) defines the number of wait states that should be inserted in each DRAM out-of-page access.

6 $\overline{RD}$ deassertion will always occur after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.

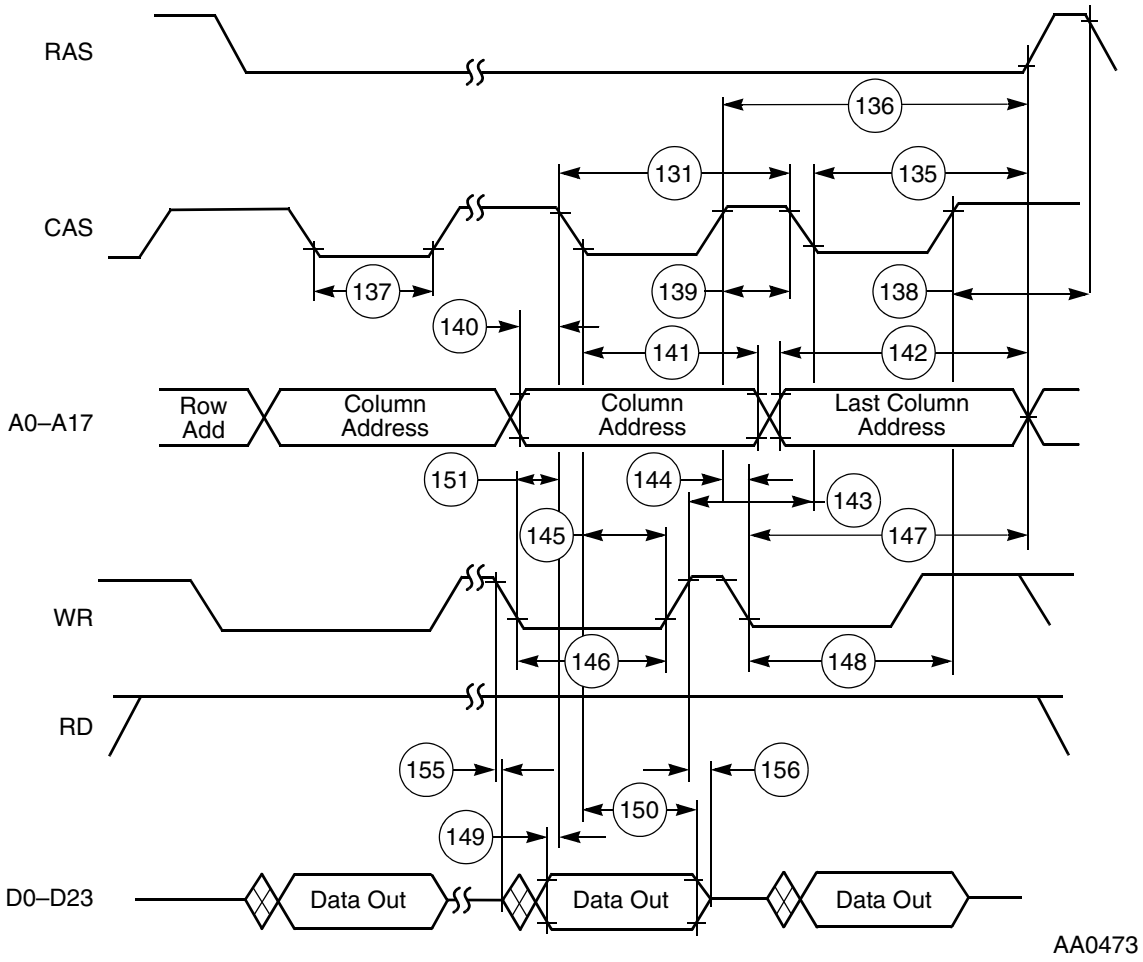


Figure 3-12 DRAM Page Mode Write Accesses

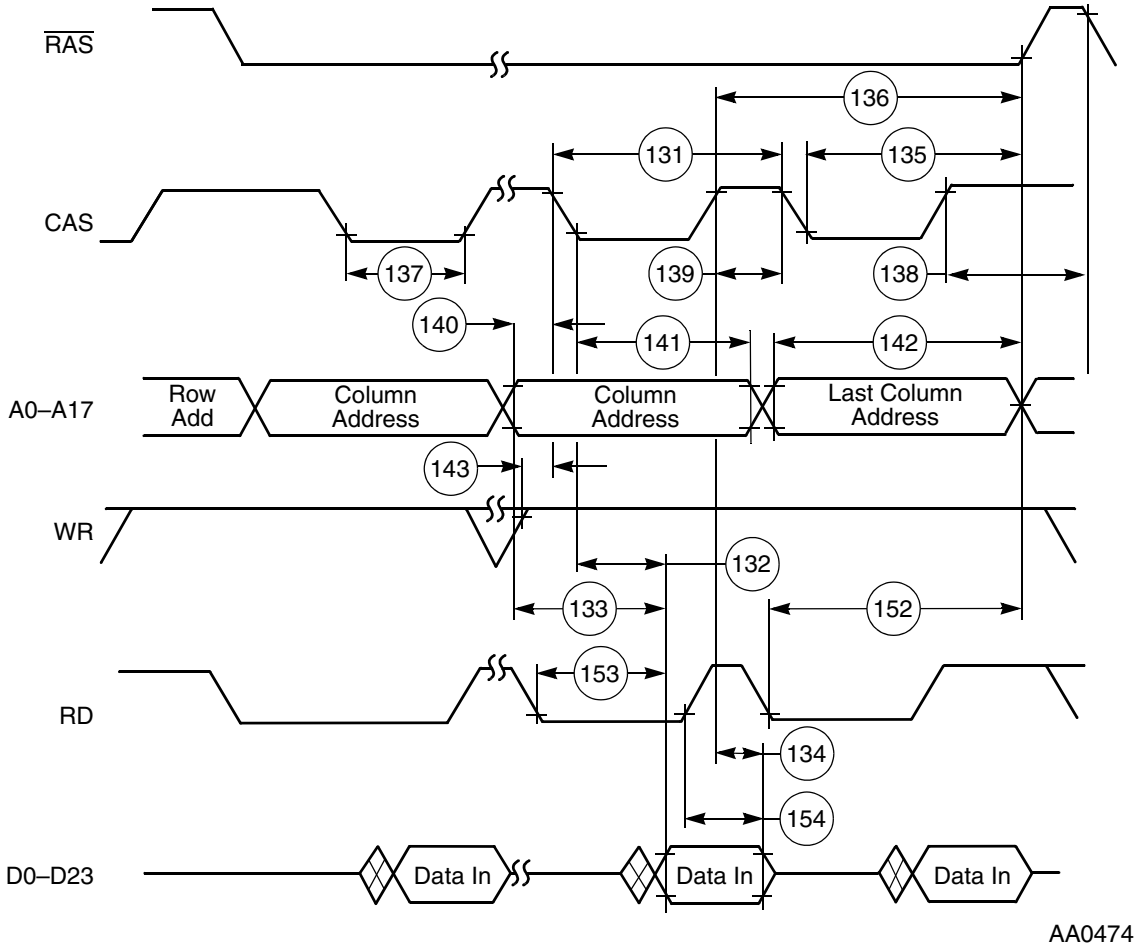


Figure 3-13 DRAM Page Mode Read Accesses

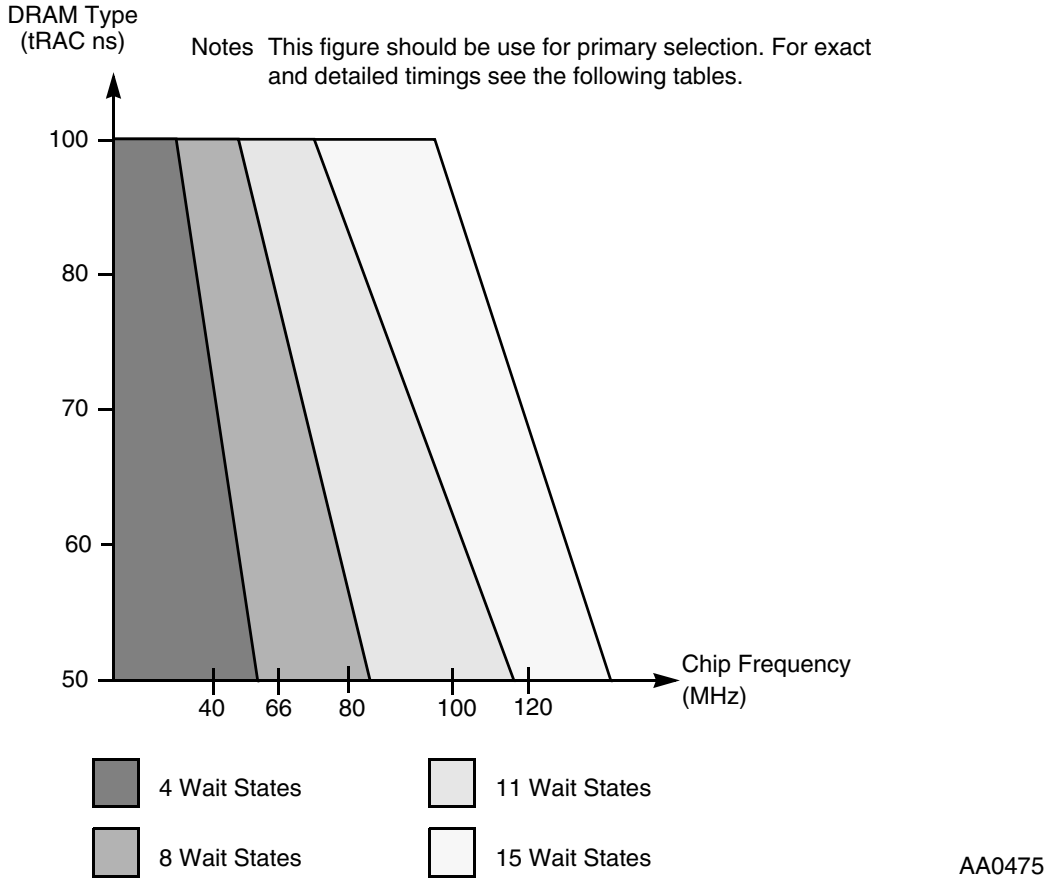


Figure 3-14 DRAM Out-of-Page Wait States Selection Guide

Table 3-13 DRAM Out-of-Page and Refresh Timings, Four Wait States[1, 2]

No.	Characteristics[3]	Symbol	Expression	20 MHz[4]		30 MHz[4]		Unit
				Min	Max	Min	Max	
157	Random read or write cycle time	t_{RC}	$5 \times T_C$	250.0	—	166.7	—	ns
158	$\overline{RAS}$ assertion to data valid (read)	t_{RAC}	$2.75 \times T_C - 7.5$	—	130.0	—	84.2	ns
159	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	$1.25 \times T_C - 7.5$	—	55.0	—	34.2	ns
160	Column address valid to data valid (read)	t_{AA}	$1.5 \times T_C - 7.5$	—	67.5	—	42.5	ns
161	$\overline{CAS}$ deassertion to data not valid (read hold time)	t_{OFF}		0.0	—	0.0	—	ns
162	$\overline{RAS}$ deassertion to $\overline{RAS}$ assertion	t_{RP}	$1.75 \times T_C - 4.0$	83.5	—	54.3	—	ns
163	$\overline{RAS}$ assertion pulse width	t_{RAS}	$3.25 \times T_C - 4.0$	158.5	—	104.3	—	ns
164	$\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$1.75 \times T_C - 4.0$	83.5	—	54.3	—	ns

Table 3-13 DRAM Out-of-Page and Refresh Timings, Four Wait States[1, 2] (continued)

No.	Characteristics[3]	Symbol	Expression	20 MHz[4]		30 MHz[4]		Unit
				Min	Max	Min	Max	
165	$\overline{RAS}$ assertion to $\overline{CAS}$ deassertion	t_{CSH}	$2.75 \times T_C - 4.0$	133.5	—	87.7	—	ns
166	$\overline{CAS}$ assertion pulse width	t_{CAS}	$1.25 \times T_C - 4.0$	58.5	—	37.7	—	ns
167	$\overline{RAS}$ assertion to $\overline{CAS}$ assertion	t_{RCD}	$1.5 \times T_C \pm 2$	73.0	77.0	48.0	52.0	ns
168	$\overline{RAS}$ assertion to column address valid	t_{RAD}	$1.25 \times T_C \pm 2$	60.5	64.5	39.7	43.7	ns
169	$\overline{CAS}$ deassertion to $\overline{RAS}$ assertion	t_{CRP}	$2.25 \times T_C - 4.0$	108.5	—	71.0	—	ns
170	$\overline{CAS}$ deassertion pulse width	t_{CP}	$1.75 \times T_C - 4.0$	83.5	—	54.3	—	ns
171	Row address valid to $\overline{RAS}$ assertion	t_{ASR}	$1.75 \times T_C - 4.0$	83.5	—	54.3	—	ns
172	$\overline{RAS}$ assertion to row address not valid	t_{RAH}	$1.25 \times T_C - 4.0$	58.5	—	37.7	—	ns
173	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	$0.25 \times T_C - 4.0$	8.5	—	4.3	—	ns
174	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$1.75 \times T_C - 4.0$	83.5	—	54.3	—	ns
175	$\overline{RAS}$ assertion to column address not valid	t_{AR}	$3.25 \times T_C - 4.0$	158.5	—	104.3	—	ns
176	Column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$2 \times T_C - 4.0$	96.0	—	62.7	—	ns
177	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$1.5 \times T_C - 3.8$	71.2	—	46.2	—	ns
178	$\overline{CAS}$ deassertion to $\overline{WR}$ assertion	t_{RCH}	$0.75 \times T_C - 3.7$	33.8	—	21.3	—	ns
179	$\overline{RAS}$ deassertion to $\overline{WR}$ assertion	t_{RRH}	$0.25 \times T_C - 3.7$	8.8	—	4.6	—	ns
180	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$1.5 \times T_C - 4.2$	70.8	—	45.8	—	ns
181	$\overline{RAS}$ assertion to $\overline{WR}$ deassertion	t_{WCR}	$3 \times T_C - 4.2$	145.8	—	95.8	—	ns
182	$\overline{WR}$ assertion pulse width	t_{WP}	$4.5 \times T_C - 4.5$	220.5	—	145.5	—	ns
183	$\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$4.75 \times T_C - 4.3$	233.2	—	154.0	—	ns
184	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	$4.25 \times T_C - 4.3$	208.2	—	137.4	—	ns
185	Data valid to $\overline{CAS}$ assertion (write)	t_{DS}	$2.25 \times T_C - 4.0$	108.5	—	71.0	—	ns
186	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$1.75 \times T_C - 4.0$	83.5	—	54.3	—	ns
187	$\overline{RAS}$ assertion to data not valid (write)	t_{DHR}	$3.25 \times T_C - 4.0$	158.5	—	104.3	—	ns
188	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$3 \times T_C - 4.3$	145.7	—	95.7	—	ns
189	$\overline{CAS}$ assertion to $\overline{RAS}$ assertion (refresh)	t_{CSR}	$0.5 \times T_C - 4.0$	21.0	—	12.7	—	ns
190	$\overline{RAS}$ deassertion to $\overline{CAS}$ assertion (refresh)	t_{RPC}	$1.25 \times T_C - 4.0$	58.5	—	37.7	—	ns

Table 3-13 DRAM Out-of-Page and Refresh Timings, Four Wait States[1, 2] (continued)

No.	Characteristics[3]	Symbol	Expression	20 MHz[4]		30 MHz[4]		Unit
				Min	Max	Min	Max	
191	$\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$4.5 \times T_C - 4.0$	221.0	—	146.0	—	ns
192	$\overline{RD}$ assertion to data valid	t_{GA}	$4 \times T_C - 7.5$	—	192.5	—	125.8	ns
193	$\overline{RD}$ deassertion to data not valid[3]	t_{GZ}		0.0	—	0.0	—	ns
194	$\overline{WR}$ assertion to data active		$0.75 \times T_C - 0.3$	37.2	—	24.7	—	ns
195	$\overline{WR}$ deassertion to data high impedance		$0.25 \times T_C$	—	12.5	—	8.3	ns

1 The number of wait states for out of page access is specified in the DCR.
2 The refresh period is specified in the DCR.
3 $\overline{RD}$ deassertion will always occur after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.
4 Reduced DSP clock speed allows use of DRAM out-of-page access with four Wait states (See Figure 3-17.).

Table 3-14 DRAM Out-of-Page and Refresh Timings, Eight Wait States[1, 2]

No.	Characteristics[3]	Symbol	Expression[4]	66 MHz		80 MHz		Unit
				Min	Max	Min	Max	
157	Random read or write cycle time	t_{RC}	$9 \times T_C$	136.4	—	112.5	—	ns
158	$\overline{RAS}$ assertion to data valid (read)	t_{RAC}	$4.75 \times T_C - 7.5$ $4.75 \times T_C - 6.5$	— —	64.5 —	— —	— 52.9	ns
159	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	$2.25 \times T_C - 7.5$ $2.25 \times T_C - 6.5$	— —	26.6 —	— —	— 21.6	ns
160	Column address valid to data valid (read)	t_{AA}	$3 \times T_C - 7.5$ $3 \times T_C - 6.5$	— —	40.0 —	— —	— 31.0	ns
161	$\overline{CAS}$ deassertion to data not valid (read hold time)	t_{OFF}		0.0	—	0.0	—	ns
162	$\overline{RAS}$ deassertion to $\overline{RAS}$ assertion	t_{RP}	$3.25 \times T_C - 4.0$	45.2	—	36.6	—	ns
163	$\overline{RAS}$ assertion pulse width	t_{RAS}	$5.75 \times T_C - 4.0$	83.1	—	67.9	—	ns
164	$\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$3.25 \times T_C - 4.0$	45.2	—	36.6	—	ns
165	$\overline{RAS}$ assertion to $\overline{CAS}$ deassertion	t_{CSH}	$4.75 \times T_C - 4.0$	68.0	—	55.5	—	ns
166	$\overline{CAS}$ assertion pulse width	t_{CAS}	$2.25 \times T_C - 4.0$	30.1	—	24.1	—	ns
167	$\overline{RAS}$ assertion to $\overline{CAS}$ assertion	t_{RCD}	$2.5 \times T_C \pm 2$	35.9	39.9	29.3	33.3	ns
168	$\overline{RAS}$ assertion to column address valid	t_{RAD}	$1.75 \times T_C \pm 2$	24.5	28.5	19.9	23.9	ns

Table 3-14 DRAM Out-of-Page and Refresh Timings, Eight Wait States[1, 2] (continued)

No.	Characteristics[3]	Symbol	Expression[4]	66 MHz		80 MHz		Unit
				Min	Max	Min	Max	
169	$\overline{CAS}$ deassertion to $\overline{RAS}$ assertion	t_{CRP}	$4.25 \times T_C - 4.0$	59.8	—	49.1	—	ns
170	$\overline{CAS}$ deassertion pulse width	t_{CP}	$2.75 \times T_C - 4.0$	37.7	—	30.4	—	ns
171	Row address valid to $\overline{RAS}$ assertion	t_{ASR}	$3.25 \times T_C - 4.0$	45.2	—	36.6	—	ns
172	$\overline{RAS}$ assertion to row address not valid	t_{RAH}	$1.75 \times T_C - 4.0$	22.5	—	17.9	—	ns
173	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	$0.75 \times T_C - 4.0$	7.4	—	5.4	—	ns
174	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$3.25 \times T_C - 4.0$	45.2	—	36.6	—	ns
175	$\overline{RAS}$ assertion to column address not valid	t_{AR}	$5.75 \times T_C - 4.0$	83.1	—	67.9	—	ns
176	Column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$4 \times T_C - 4.0$	56.6	—	46.0	—	ns
177	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$2 \times T_C - 3.8$	26.5	—	21.2	—	ns
178	$\overline{CAS}$ deassertion to $\overline{WR}$[5] assertion	t_{RCH}	$1.25 \times T_C - 3.7$	15.2	—	11.9	—	ns
179	$\overline{RAS}$ deassertion to $\overline{WR}$[5] assertion	t_{RRH}	$0.25 \times T_C - 3.7$ $0.25 \times T_C - 3.0$	0.1 —	— —	— 0.1	— —	ns
180	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$3 \times T_C - 4.2$	41.3	—	33.3	—	ns
181	$\overline{RAS}$ assertion to $\overline{WR}$ deassertion	t_{WCR}	$5.5 \times T_C - 4.2$	79.1	—	64.6	—	ns
182	$\overline{WR}$ assertion pulse width	t_{WP}	$8.5 \times T_C - 4.5$	124.3	—	101.8	—	ns
183	$\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$8.75 \times T_C - 4.3$	128.3	—	105.1	—	ns
184	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	$7.75 \times T_C - 4.3$	113.1	—	92.6	—	ns
185	Data valid to $\overline{CAS}$ assertion (write)	t_{DS}	$4.75 \times T_C - 4.0$	68.0	—	55.4	—	ns
186	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$3.25 \times T_C - 4.0$	45.2	—	36.6	—	ns
187	$\overline{RAS}$ assertion to data not valid (write)	t_{DHR}	$5.75 \times T_C - 4.0$	83.1	—	67.9	—	ns
188	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$5.5 \times T_C - 4.3$	79.0	—	64.5	—	ns
189	$\overline{CAS}$ assertion to $\overline{RAS}$ assertion (refresh)	t_{CSR}	$1.5 \times T_C - 4.0$	18.7	—	14.8	—	ns
190	$\overline{RAS}$ deassertion to $\overline{CAS}$ assertion (refresh)	t_{RPC}	$1.75 \times T_C - 4.0$	22.5	—	17.9	—	ns
191	$\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$8.5 \times T_C - 4.0$	124.8	—	102.3	—	ns
192	$\overline{RD}$ assertion to data valid	t_{GA}	$7.5 \times T_C - 7.5$ $7.5 \times T_C - 6.5$	— —	106.1 —	— —	— 87.3	ns

Table 3-14 DRAM Out-of-Page and Refresh Timings, Eight Wait States[1, 2] (continued)

No.	Characteristics[3]	Symbol	Expression[4]	66 MHz		80 MHz		Unit
				Min	Max	Min	Max	
193	$\overline{RD}$ deassertion to data not valid[4]	t_{GZ}	0.0	0.0	—	0.0	—	ns
194	$\overline{WR}$ assertion to data active		$0.75 \times T_C - 0.3$	11.1	—	9.1	—	ns
195	$\overline{WR}$ deassertion to data high impedance		$0.25 \times T_C$	—	3.8	—	3.1	ns

1 The number of wait states for out-of-page access is specified in the DCR.
2 The refresh period is specified in the DCR.
3 $\overline{RD}$ deassertion will always occur after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.
4 The asynchronous delays specified in the expressions are valid for DSP56366.
5 Either t_{RCH} or t_{RRH} must be satisfied for read cycles.

Table 3-15 DRAM Out-of-Page and Refresh Timings, Eleven Wait States[1, 2]

No.	Characteristics[3]	Symbol	Expression[4]	Min	Max	Unit
157	Random read or write cycle time	t_{RC}	$12 \times T_C$	120.0	—	ns
158	$\overline{RAS}$ assertion to data valid (read)	t_{RAC}	$6.25 \times T_C - 7.0$	—	55.5	ns
159	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	$3.75 \times T_C - 7.0$	—	30.5	ns
160	Column address valid to data valid (read)	t_{AA}	$4.5 \times T_C - 7.0$	—	38.0	ns
161	$\overline{CAS}$ deassertion to data not valid (read hold time)	t_{OFF}		0.0	—	ns
162	$\overline{RAS}$ deassertion to $\overline{RAS}$ assertion	t_{RP}	$4.25 \times T_C - 4.0$	38.5	—	ns
163	$\overline{RAS}$ assertion pulse width	t_{RAS}	$7.75 \times T_C - 4.0$	73.5	—	ns
164	$\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$5.25 \times T_C - 4.0$	48.5	—	ns
165	$\overline{RAS}$ assertion to $\overline{CAS}$ deassertion	t_{CSH}	$6.25 \times T_C - 4.0$	58.5	—	ns
166	$\overline{CAS}$ assertion pulse width	t_{CAS}	$3.75 \times T_C - 4.0$	33.5	—	ns
167	$\overline{RAS}$ assertion to $\overline{CAS}$ assertion	t_{RCD}	$2.5 \times T_C \pm 4.0$	21.0	29.0	ns
168	$\overline{RAS}$ assertion to column address valid	t_{RAD}	$1.75 \times T_C \pm 4.0$	13.5	21.5	ns
169	$\overline{CAS}$ deassertion to $\overline{RAS}$ assertion	t_{CRP}	$5.75 \times T_C - 4.0$	53.5	—	ns
170	$\overline{CAS}$ deassertion pulse width	t_{CP}	$4.25 \times T_C - 4.0$	38.5	—	ns
171	Row address valid to $\overline{RAS}$ assertion	t_{ASR}	$4.25 \times T_C - 4.0$	38.5	—	ns
172	$\overline{RAS}$ assertion to row address not valid	t_{RAH}	$1.75 \times T_C - 4.0$	13.5	—	ns
173	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	$0.75 \times T_C - 4.0$	3.5	—	ns

Table 3-15 DRAM Out-of-Page and Refresh Timings, Eleven Wait States[1, 2] (continued)

No.	Characteristics[3]	Symbol	Expression[4]	Min	Max	Unit
174	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$5.25 \times T_C - 4.0$	48.5	—	ns
175	$\overline{RAS}$ assertion to column address not valid	t_{AR}	$7.75 \times T_C - 4.0$	73.5	—	ns
176	Column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$6 \times T_C - 4.0$	56.0	—	ns
177	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$3.0 \times T_C - 4.0$	26.0	—	ns
178	$\overline{CAS}$ deassertion to $\overline{WR}$[5] assertion	t_{RCH}	$1.75 \times T_C - 4.0$	13.5	—	ns
179	$\overline{RAS}$ deassertion to $\overline{WR}$[5] assertion	t_{RRH}	$0.25 \times T_C - 2.0$	0.5	—	ns
180	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$5 \times T_C - 4.2$	45.8	—	ns
181	$\overline{RAS}$ assertion to $\overline{WR}$ deassertion	t_{WCR}	$7.5 \times T_C - 4.2$	70.8	—	ns
182	$\overline{WR}$ assertion pulse width	t_{WP}	$11.5 \times T_C - 4.5$	110.5	—	ns
183	$\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$11.75 \times T_C - 4.3$	113.2	—	ns
184	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	$10.25 \times T_C - 4.3$	103.2	—	ns
185	Data valid to $\overline{CAS}$ assertion (write)	t_{DS}	$5.75 \times T_C - 4.0$	53.5	—	ns
186	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$5.25 \times T_C - 4.0$	48.5	—	ns
187	$\overline{RAS}$ assertion to data not valid (write)	t_{DHR}	$7.75 \times T_C - 4.0$	73.5	—	ns
188	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$6.5 \times T_C - 4.3$	60.7	—	ns
189	$\overline{CAS}$ assertion to $\overline{RAS}$ assertion (refresh)	t_{CSR}	$1.5 \times T_C - 4.0$	11.0	—	ns
190	$\overline{RAS}$ deassertion to $\overline{CAS}$ assertion (refresh)	t_{RPC}	$2.75 \times T_C - 4.0$	23.5	—	ns
191	$\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$11.5 \times T_C - 4.0$	111.0	—	ns
192	$\overline{RD}$ assertion to data valid	t_{GA}	$10 \times T_C - 7.0$	—	93.0	ns
193	$\overline{RD}$ deassertion to data not valid[3]	t_{GZ}		0.0	—	ns
194	$\overline{WR}$ assertion to data active		$0.75 \times T_C - 0.3$	7.2	—	ns
195	$\overline{WR}$ deassertion to data high impedance		$0.25 \times T_C$	—	2.5	ns

1 The number of wait states for out-of-page access is specified in the DCR.

2 The refresh period is specified in the DCR.

3 $\overline{RD}$ deassertion will always occur after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.

4 The asynchronous delays specified in the expressions are valid for DSP56366.

5 Either t_{RCH} or t_{RRH} must be satisfied for read cycles.

Table 3-16 DRAM Out-of-Page and Refresh Timings, Fifteen Wait States[1, 2]

No.	Characteristics[3]	Symbol	Expression	Min	Max	Unit
157	Random read or write cycle time	t_{RC}	$16 \times T_C$	133.3	—	ns
158	$\overline{RAS}$ assertion to data valid (read)	t_{RAC}	$8.25 \times T_C - 5.7$	—	63.0	ns
159	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	$4.75 \times T_C - 5.7$	—	33.9	ns
160	Column address valid to data valid (read)	t_{AA}	$5.5 \times T_C - 5.7$	—	40.1	ns
161	$\overline{CAS}$ deassertion to data not valid (read hold time)	t_{OFF}	0.0	0.0	—	ns
162	$\overline{RAS}$ deassertion to $\overline{RAS}$ assertion	t_{RP}	$6.25 \times T_C - 4.0$	48.1	—	ns
163	$\overline{RAS}$ assertion pulse width	t_{RAS}	$9.75 \times T_C - 4.0$	77.2	—	ns
164	$\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$6.25 \times T_C - 4.0$	48.1	—	ns
165	$\overline{RAS}$ assertion to $\overline{CAS}$ deassertion	t_{CSH}	$8.25 \times T_C - 4.0$	64.7	—	ns
166	$\overline{CAS}$ assertion pulse width	t_{CAS}	$4.75 \times T_C - 4.0$	35.6	—	ns
167	$\overline{RAS}$ assertion to $\overline{CAS}$ assertion	t_{RCD}	$3.5 \times T_C \pm 2$	27.2	31.2	ns
168	$\overline{RAS}$ assertion to column address valid	t_{RAD}	$2.75 \times T_C \pm 2$	20.9	24.9	ns
169	$\overline{CAS}$ deassertion to $\overline{RAS}$ assertion	t_{CRP}	$7.75 \times T_C - 4.0$	60.6	—	ns
170	$\overline{CAS}$ deassertion pulse width	t_{CP}	$6.25 \times T_C - 4.0$	48.1	—	ns
171	Row address valid to $\overline{RAS}$ assertion	t_{ASR}	$6.25 \times T_C - 4.0$	48.1	—	ns
172	$\overline{RAS}$ assertion to row address not valid	t_{RAH}	$2.75 \times T_C - 4.0$	18.9	—	ns
173	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	$0.75 \times T_C - 4.0$	2.2	—	ns
174	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$6.25 \times T_C - 4.0$	48.1	—	ns
175	$\overline{RAS}$ assertion to column address not valid	t_{AR}	$9.75 \times T_C - 4.0$	77.2	—	ns
176	Column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$7 \times T_C - 4.0$	54.3	—	ns
177	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$5 \times T_C - 3.8$	37.9	—	ns
178	$\overline{CAS}$ deassertion to $\overline{WR}$[4] assertion	t_{RCH}	$1.75 \times T_C - 3.7$	10.9	—	ns
179	$\overline{RAS}$ deassertion to $\overline{WR}$[5] assertion	t_{RRH}	$0.25 \times T_C - 2.0$	0.1	—	ns
180	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$6 \times T_C - 4.2$	45.8	—	ns
181	$\overline{RAS}$ assertion to $\overline{WR}$ deassertion	t_{WCR}	$9.5 \times T_C - 4.2$	75.0	—	ns
182	$\overline{WR}$ assertion pulse width	t_{WP}	$15.5 \times T_C - 4.5$	124.7	—	ns
183	$\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$15.75 \times T_C - 4.3$	126.9	—	ns

Table 3-16 DRAM Out-of-Page and Refresh Timings, Fifteen Wait States[1, 2] (continued)

No.	Characteristics[3]	Symbol	Expression	Min	Max	Unit
184	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	$14.25 \times T_C - 4.3$	114.4	—	ns
185	Data valid to $\overline{CAS}$ assertion (write)	t_{DS}	$8.75 \times T_C - 4.0$	68.9	—	ns
186	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$6.25 \times T_C - 4.0$	48.1	—	ns
187	$\overline{RAS}$ assertion to data not valid (write)	t_{DHR}	$9.75 \times T_C - 4.0$	77.2	—	ns
188	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$9.5 \times T_C - 4.3$	74.9	—	ns
189	$\overline{CAS}$ assertion to $\overline{RAS}$ assertion (refresh)	t_{CSR}	$1.5 \times T_C - 4.0$	8.5	—	ns
190	$\overline{RAS}$ deassertion to $\overline{CAS}$ assertion (refresh)	t_{RPC}	$4.75 \times T_C - 4.0$	35.6	—	ns
191	$\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$15.5 \times T_C - 4.0$	125.2	—	ns
192	$\overline{RD}$ assertion to data valid	t_{GA}	$14 \times T_C - 5.7$	—	111.0	ns
193	$\overline{RD}$ deassertion to data not valid[3]	t_{GZ}		0.0	—	ns
194	$\overline{WR}$ assertion to data active		$0.75 \times T_C - 0.3$	5.9	—	ns
195	$\overline{WR}$ deassertion to data high impedance		$0.25 \times T_C$	—	2.1	ns

1 The number of wait states for out-of-page access is specified in the DCR.
2 The refresh period is specified in the DCR.
3 $\overline{RD}$ deassertion will always occur after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.
4 Either t_{RCH} or t_{RRH} must be satisfied for read cycles.

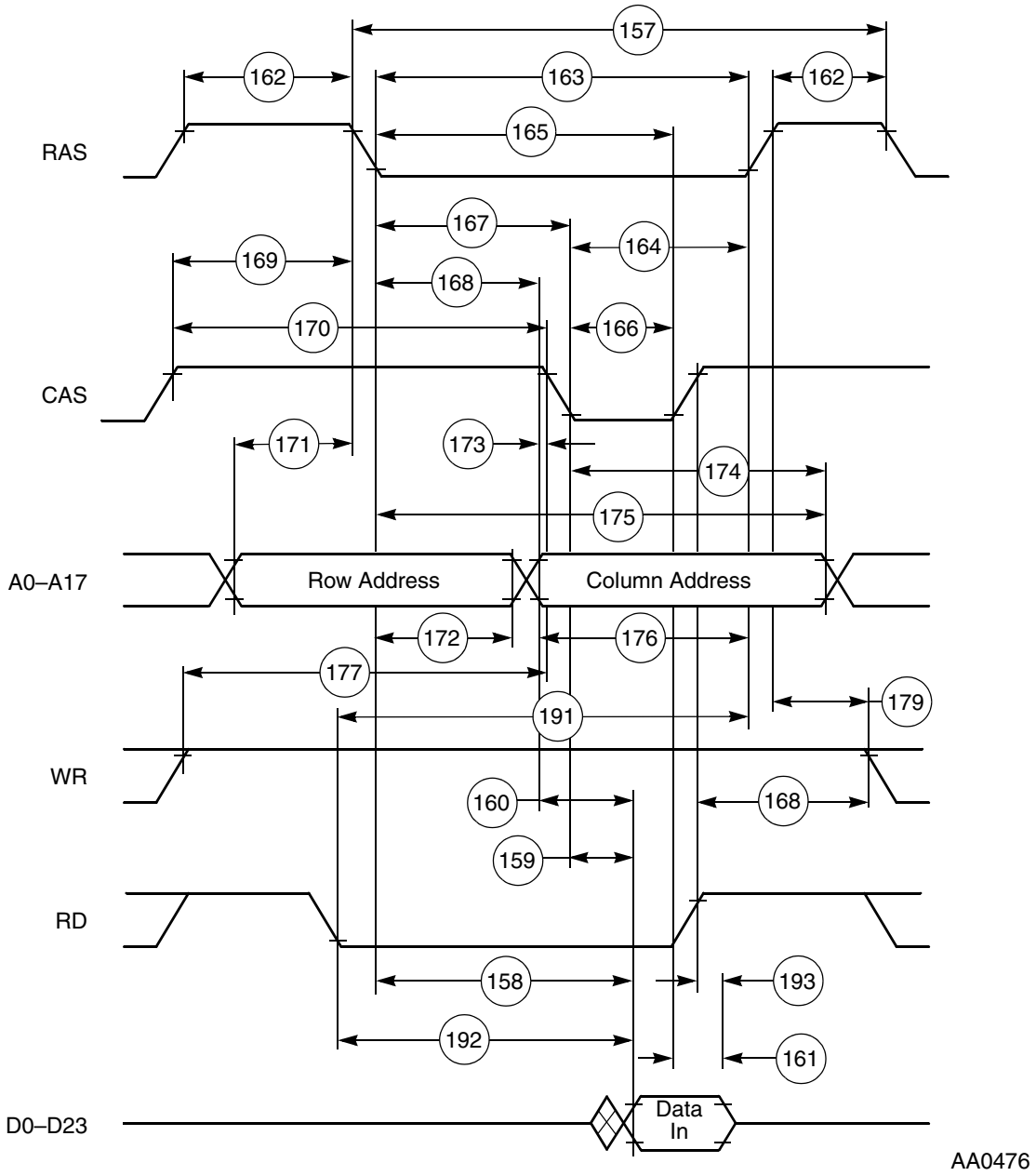


Figure 3-15 DRAM Out-of-Page Read Access

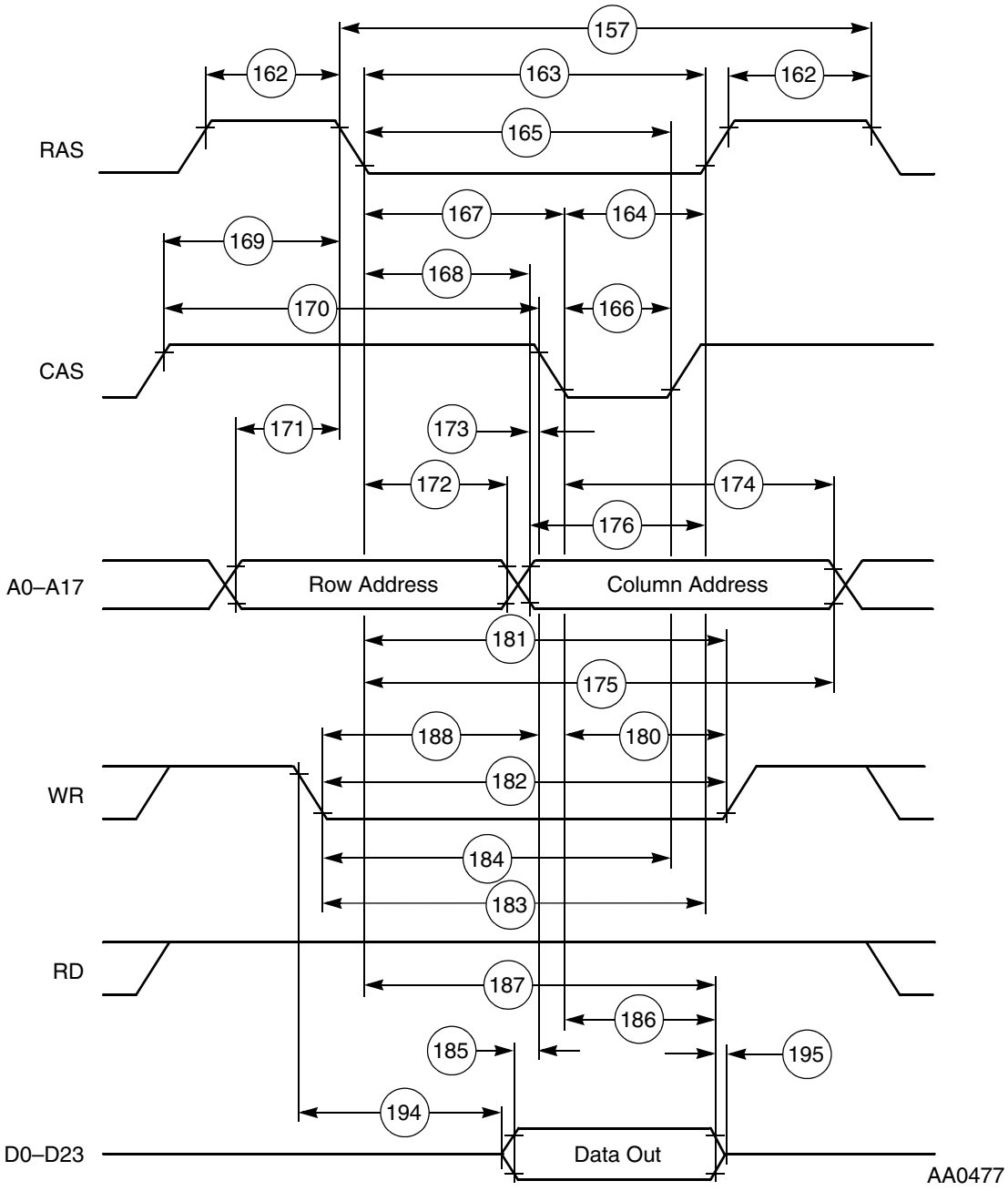


Figure 3-16 DRAM Out-of-Page Write Access

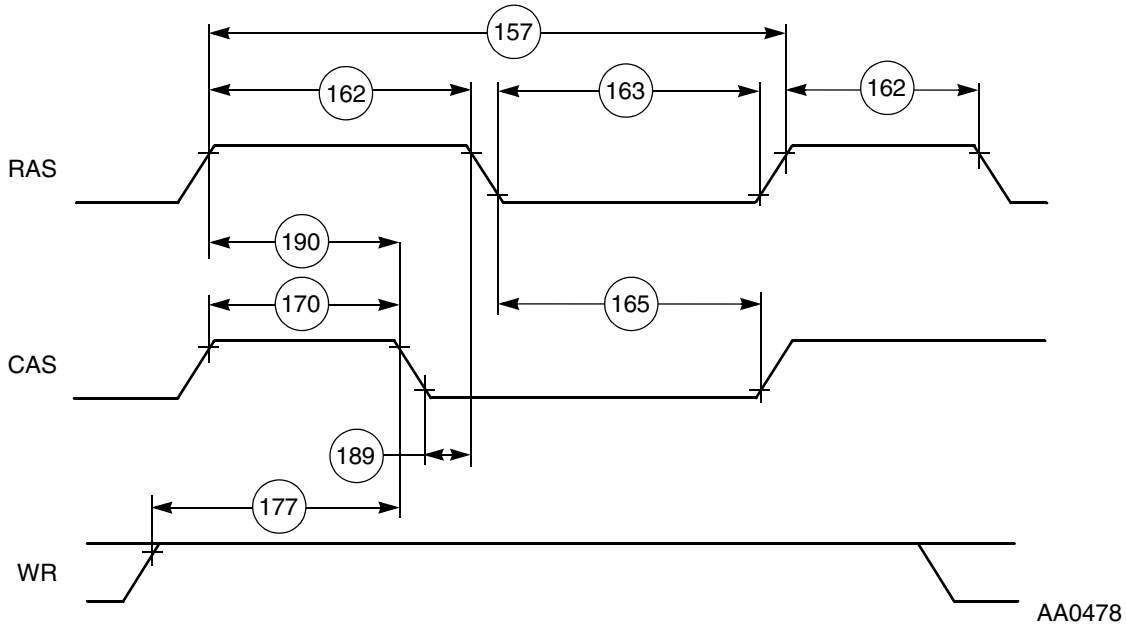


Figure 3-17 DRAM Refresh Access

3.10.3 Arbitration Timings

Table 3-17 Asynchronous Bus Arbitration timing

No.	Characteristics	Expression	120 MHz		Unit
			Min	Max	
250	$\overline{BB}$ assertion window from $\overline{BG}$ input negation.	2 .5* Tc + 5	—	25.8	ns
251	Delay from $\overline{BB}$ assertion to $\overline{BG}$ assertion	2 * Tc + 5	21.7	—	ns

Notes:
1. Bit 13 in the OMR register must be set to enter Asynchronous Arbitration mode
2. If Asynchronous Arbitration mode is active, none of the timings in Table 3-17 is required.
3. In order to guarantee timings 250, and 251, it is recommended to assert $\overline{BG}$ inputs to different 56300 devices (on the same bus) in a non overlap manner as shown in Figure 3-18.

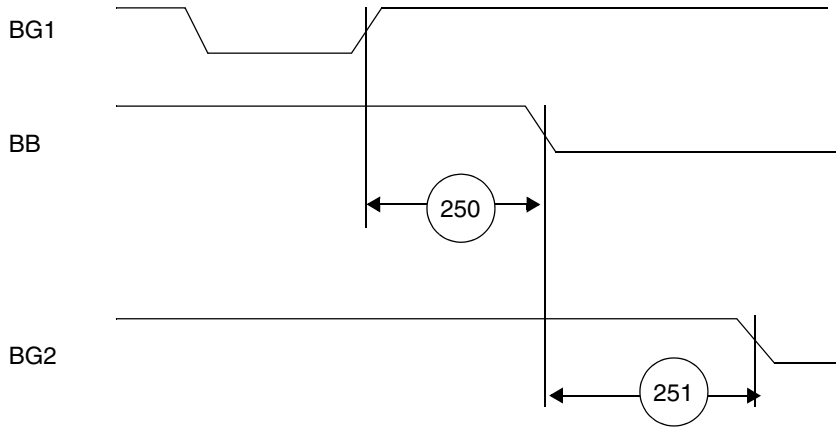


Figure 3-18 Asynchronous Bus Arbitration Timing

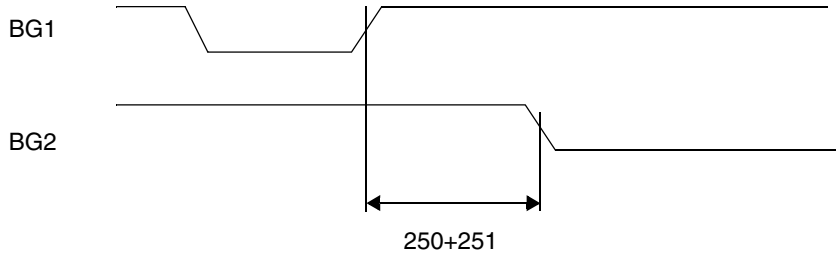


Figure 3-19 Asynchronous Bus Arbitration Timing

Background explanation for Asynchronous Bus Arbitration:

The asynchronous bus arbitration is enabled by internal synchronization circuits on $\overline{BG}$ and $\overline{BB}$ inputs. These synchronization circuits add delay from the external signal until it is exposed to internal logic. As a result of this delay, a 56300 part may assume mastership and assert $\overline{BB}$ for some time after $\overline{BG}$ is negated. This is the reason for timing 250.

Once $\overline{BB}$ is asserted, there is a synchronization delay from $\overline{BB}$ assertion to the time this assertion is exposed to other 56300 components which are potential masters on the same bus. If $\overline{BG}$ input is asserted before that time, a situation of $\overline{BG}$ asserted, and $\overline{BB}$ negated, may cause another 56300 component to assume mastership at the same time. Therefore some non-overlap period between one $\overline{BG}$ input active to another $\overline{BG}$ input active is required. Timing 251 ensures that such a situation is avoided.

3.11 Parallel Host Interface (HDI08) Timing

Table 3-18 Host Interface (HDI08) Timing[1, 2]

No.	Characteristics[3]	Expression	120 MHz		Unit
			Min	Max	
317	Read data strobe assertion width[4] $\overline{\text{HACK}}$ read assertion width	$T_C + 9.9$	18.3	—	ns
318	Read data strobe deassertion width[4] $\overline{\text{HACK}}$ read deassertion width	—	9.9	—	ns
319	Read data strobe deassertion width[4] after "Last Data Register" reads[5,6], or between two consecutive CVR, ICR, or ISR reads[7] $\overline{\text{HACK}}$ deassertion width after "Last Data Register" reads[5,6]	$2.5 \times T_C + 6.6$	27.4	—	ns
320	Write data strobe assertion width[8] $\overline{\text{HACK}}$ write assertion width	—	13.2	—	ns
321	Write data strobe deassertion width[8] $\overline{\text{HACK}}$ write deassertion width • after ICR, CVR and "Last Data Register" writes[5] • after IVR writes, or • after TXH:TXM writes (with HBE=0), or • after TXL:TXM writes (with HBE=1)	$2.5 \times T_C + 6.6$	27.4 16.5	— —	ns
322	$\overline{\text{HAS}}$ assertion width	—	9.9	—	ns
323	$\overline{\text{HAS}}$ deassertion to data strobe assertion[9]	—	0.0	—	ns
324	Host data input setup time before write data strobe deassertion[8] Host data input setup time before $\overline{\text{HACK}}$ write deassertion	—	9.9	—	ns
325	Host data input hold time after write data strobe deassertion[8] Host data input hold time after $\overline{\text{HACK}}$ write deassertion	—	3.3	—	ns
326	Read data strobe assertion to output data active from high impedance[4] $\overline{\text{HACK}}$ read assertion to output data active from high impedance	—	3.3	—	ns
327	Read data strobe assertion to output data valid[4] $\overline{\text{HACK}}$ read assertion to output data valid	—	—	24.2	ns
328	Read data strobe deassertion to output data high impedance[4] $\overline{\text{HACK}}$ read deassertion to output data high impedance	—	—	9.9	ns
329	Output data hold time after read data strobe deassertion[4] Output data hold time after $\overline{\text{HACK}}$ read deassertion	—	3.3	—	ns
330	HCS assertion to read data strobe deassertion[4]	$T_C + 9.9$	18.2	—	ns
331	$\overline{\text{HCS}}$ assertion to write data strobe deassertion[8]	—	9.9	—	ns
332	$\overline{\text{HCS}}$ assertion to output data valid	—	—	19.1	ns

Table 3-18 Host Interface (HDI08) Timing[1, 2] (continued)

No.	Characteristics[3]	Expression	120 MHz		Unit
			Min	Max	
333	$\overline{HCS}$ hold time after data strobe deassertion[9]	—	0.0	—	ns
334	Address (AD7–AD0) setup time before $\overline{HAS}$ deassertion (HMUX=1)	—	4.7	—	ns
335	Address (AD7–AD0) hold time after $\overline{HAS}$ deassertion (HMUX=1)	—	3.3	—	ns
336	A10–A8 (HMUX=1), A2–A0 (HMUX=0), HR/$\overline{W}$ setup time before data strobe assertion[9] • Read • Write	—	0 4.7	— —	ns
337	A10–A8 (HMUX=1), A2–A0 (HMUX=0), HR/$\overline{W}$ hold time after data strobe deassertion[9]	—	3.3	—	ns
338	Delay from read data strobe deassertion to host request assertion for “Last Data Register” read[4, 5, 10]	T_C	8.3	—	ns
339	Delay from write data strobe deassertion to host request assertion for “Last Data Register” write[5, 8, 10]	$2 \times T_C$	16.7	—	ns
340	Delay from data strobe assertion to host request deassertion for “Last Data Register” read or write (HROD = 0)[5, 9, 10]	—	—	19.1	ns
341	Delay from data strobe assertion to host request deassertion for “Last Data Register” read or write (HROD = 1, open drain Host Request)[5, 9, 10, 11]	—	—	300.0	ns
342	Delay from DMA $\overline{HACK}$ deassertion to HOREQ assertion • For “Last Data Register” read[5] • For “Last Data Register” write[5] • For other cases	 $2 \times T_C + 19.1$ $1.5 \times T_C + 19.1$	 35.8 31.6 0.0	 — — —	ns
343	Delay from DMA $\overline{HACK}$ assertion to HOREQ deassertion • HROD = 0[5]	—	—	20.2	ns
344	Delay from DMA $\overline{HACK}$ assertion to HOREQ deassertion for “Last Data Register” read or write • HROD = 1, open drain Host Request[5, 11]	—	—	300.0	ns

1 See Host Port Usage Considerations in the DSP56366 User’s Manual.

2 In the timing diagrams below, the controls pins are drawn as active low. The pin polarity is programmable.

3 V_{CC} = 3.3 V ± 0.16 V; T_J = –40°C to +110°C, C_L = 50 pF

4 The read data strobe is HRD in the dual data strobe mode and HDS in the single data strobe mode.

5 The “last data register” is the register at address $7, which is the last location to be read or written in data transfers.

6 This timing is applicable only if a read from the “last data register” is followed by a read from the RXL, RXM, or RXH registers without first polling RXDF or HREQ bits, or waiting for the assertion of the HOREQ signal.

7 This timing is applicable only if two consecutive reads from one of these registers are executed.

8 The write data strobe is HWR in the dual data strobe mode and HDS in the single data strobe mode.

9 The data strobe is host read (HRD) or host write (HWR) in the dual data strobe mode and host data strobe (HDS) in the single data strobe mode.

10 The host request is HOREQ in the single host request mode and HRRQ and HTRQ in the double host request mode.

11 In this calculation, the host request signal is pulled up by a 4.7 kΩ resistor in the open-drain mode.

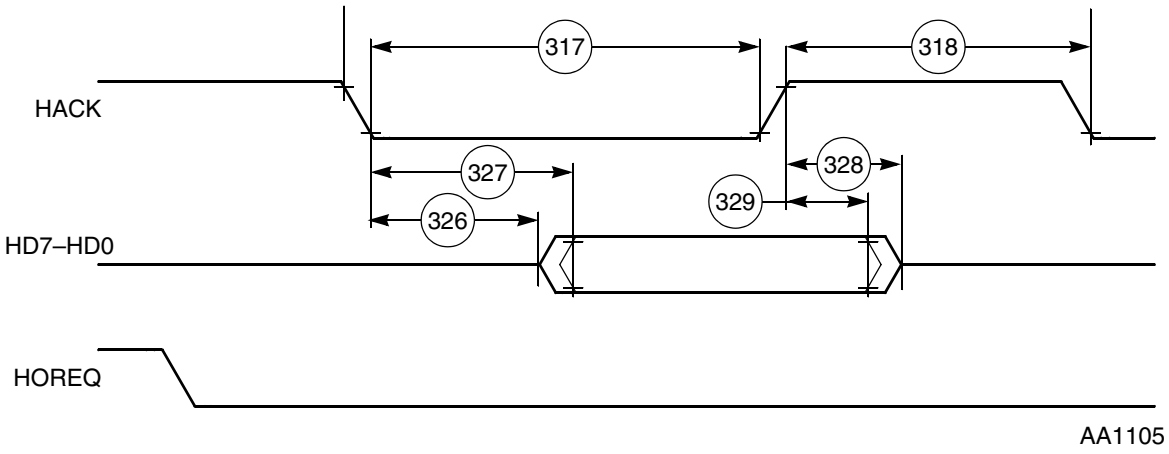


Figure 3-20 Host Interrupt Vector Register (IVR) Read Timing Diagram

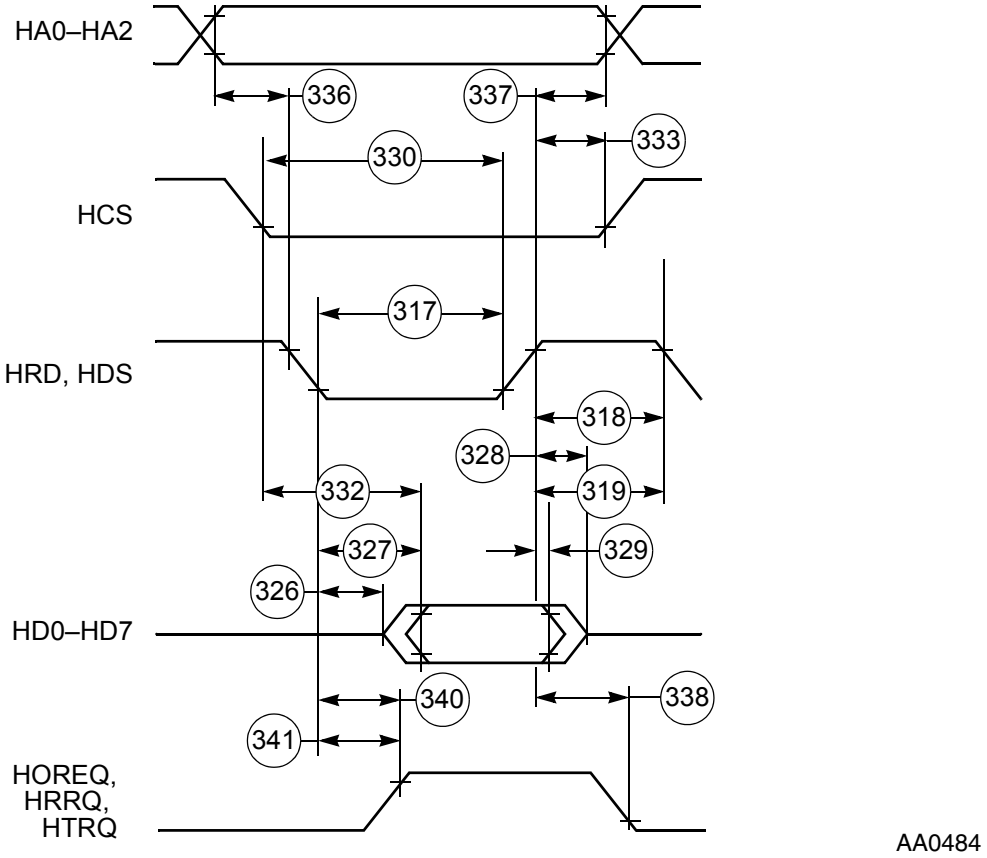


Figure 3-21 Read Timing Diagram, Non-Multiplexed Bus

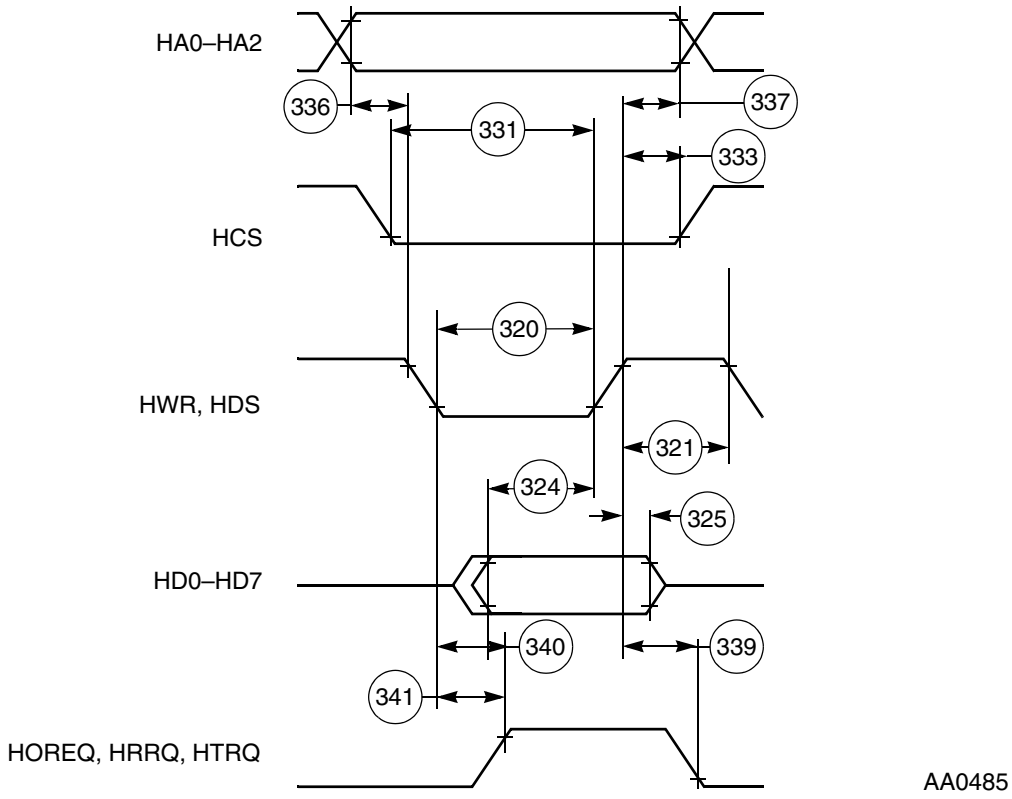


Figure 3-22 Write Timing Diagram, Non-Multiplexed Bus

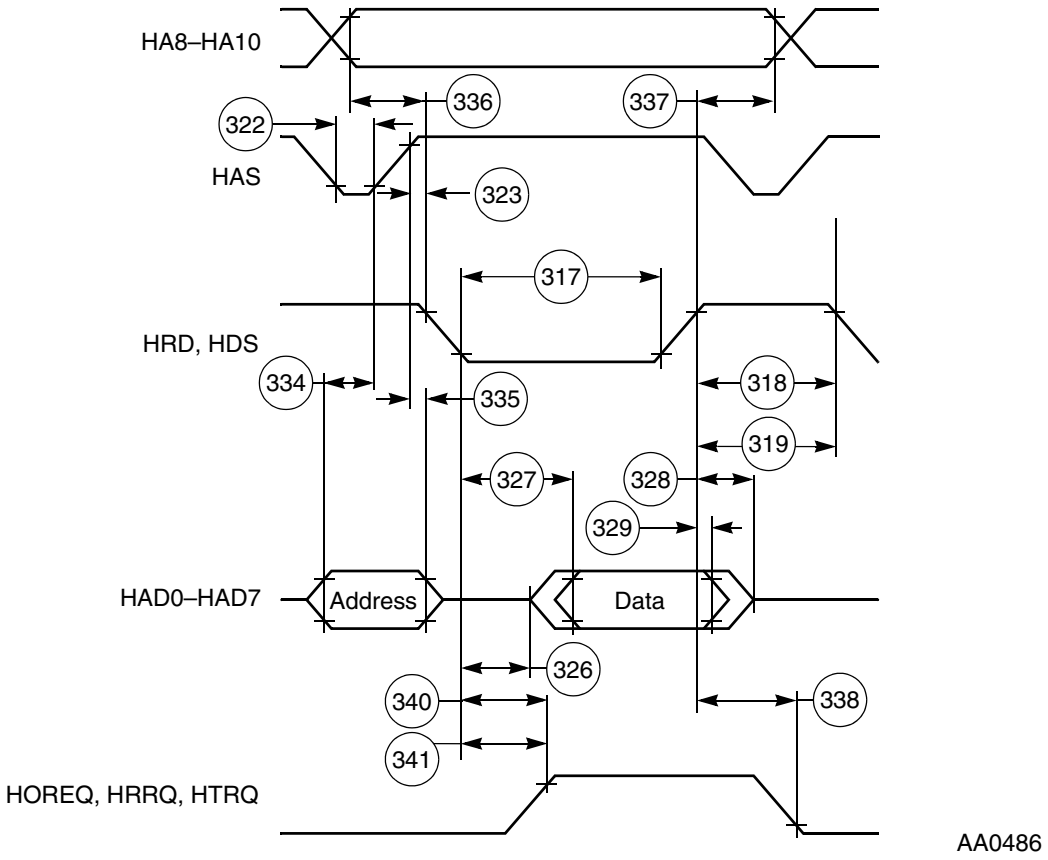


Figure 3-23 Read Timing Diagram, Multiplexed Bus

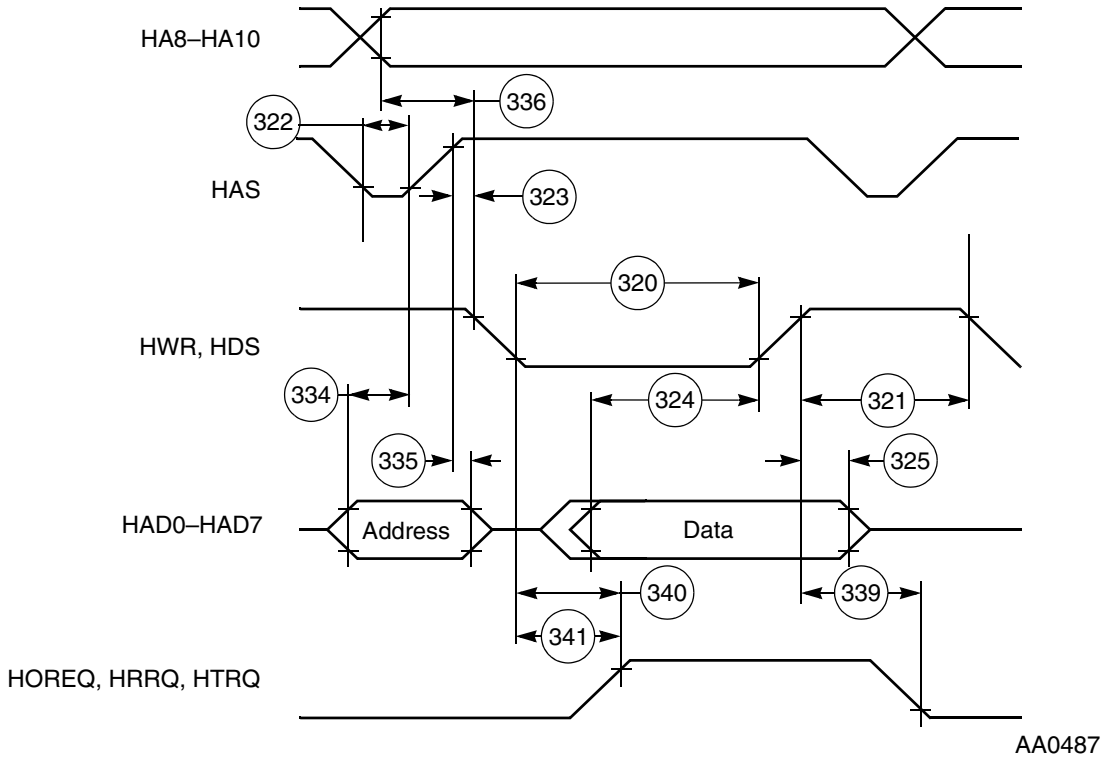


Figure 3-24 Write Timing Diagram, Multiplexed Bus

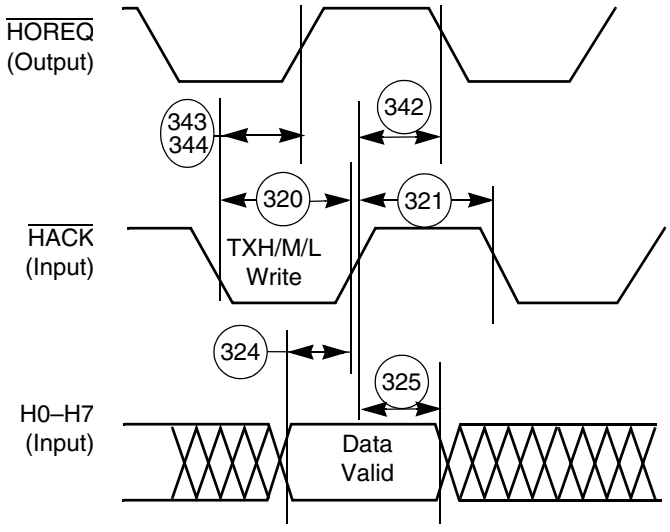


Figure 3-25 Host DMA Write Timing Diagram

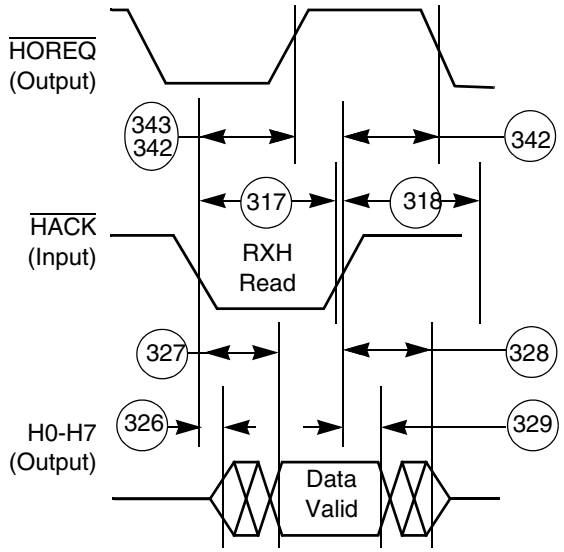


Figure 3-26 Host DMA Read Timing Diagram

3.12 Serial Host Interface SPI Protocol Timing

Table 3-19 Serial Host Interface SPI Protocol Timing

No.	Characteristics[1]	Mode	Filter Mode	Expression	Min	Max	Unit
140	Tolerable spike width on clock or data in	—	Bypassed	—	—	0	ns
			Narrow	—	—	50	ns
			Wide	—	—	100	ns
141	Minimum serial clock cycle = t_{SPICC}(min)	Master	Bypassed	$6\times T_C+46$	96	—	ns
			Narrow	$6\times T_C+152$	202	—	ns
			Wide	$6\times T_C+223$	273	—	ns
142	Serial clock high period	Master	Bypassed	$0.5\times t_{SPICC}-10$	38	—	ns
			Narrow	$0.5\times t_{SPICC}-10$	91	—	ns
			Wide	$0.5\times t_{SPICC}-10$	126.5	—	ns
		Slave	Bypassed	$2.5\times T_C+12$	32.8	—	ns
			Narrow	$2.5\times T_C+102$	122.8	—	ns
			Wide	$2.5\times T_C+189$	209.8	—	ns

Table 3-19 Serial Host Interface SPI Protocol Timing (continued)

No.	Characteristics[1]	Mode	Filter Mode	Expression	Min	Max	Unit
143	Serial clock low period	Master	Bypassed	$0.5 \times t_{SPICC} - 10$	38	—	ns
			Narrow	$0.5 \times t_{SPICC} - 10$	91	—	ns
			Wide	$0.5 \times t_{SPICC} - 10$	126.5	—	ns
		Slave	Bypassed	$2.5 \times T_C + 12$	32.8	—	ns
			Narrow	$2.5 \times T_C + 102$	122.8	—	ns
			Wide	$2.5 \times T_C + 189$	209.8	—	ns
144	Serial clock rise/fall time	Master	—	—	—	10	ns
		Slave	—	—	—	2000	ns
146	$\overline{SS}$ assertion to first SCK edge CPHA = 0	Slave	Bypassed	$3.5 \times T_C + 15$	44.2	—	ns
			Narrow	0	0	—	ns
			Wide	0	0	—	ns
	CPHA = 1	Slave	Bypassed	10	10	—	ns
			Narrow	0	0	—	ns
			Wide	0	0	—	ns
147	Last SCK edge to $\overline{SS}$ not asserted	Slave	Bypassed	12	12	—	ns
			Narrow	102	102	—	ns
			Wide	189	189	—	ns
148	Data input valid to SCK edge (data input set-up time)	Master/Slave	Bypassed	0	0	—	ns
			Narrow	$MAX\{(20-T_C), 0\}$	11.7	—	ns
			Wide	$MAX\{(40-T_C), 0\}$	31.7	—	ns
149	SCK last sampling edge to data input not valid	Master/Slave	Bypassed	$2.5 \times T_C + 10$	30.8	—	ns
			Narrow	$2.5 \times T_C + 30$	50.8	—	ns
			Wide	$2.5 \times T_C + 50$	70.8	—	ns
150	$\overline{SS}$ assertion to data out active	Slave	—	2	2	—	ns
151	$\overline{SS}$ deassertion to data high impedance[2]	Slave	—	9	—	9	ns

Table 3-19 Serial Host Interface SPI Protocol Timing (continued)

No.	Characteristics[1]	Mode	Filter Mode	Expression	Min	Max	Unit
152	SCK edge to data out valid (data out delay time)	Master/Slave	Bypassed	$2\times T_C+33$	—	49.7	ns
			Narrow	$2\times T_C+123$	—	139.7	ns
			Wide	$2\times T_C+210$	—	226.7	ns
153	SCK edge to data out not valid (data out hold time)	Master/Slave	Bypassed	T_C+5	13.3	—	ns
			Narrow	T_C+55	63.3	—	ns
			Wide	T_C+106	114.3	—	ns
154	$\overline{SS}$ assertion to data out valid (CPHA = 0)	Slave	—	T_C+33	—	41.3	ns
157	First SCK sampling edge to $\overline{HREQ}$ output deassertion	Slave	Bypassed	$2.5\times T_C+30$	—	50.8	ns
			Narrow	$2.5\times T_C+120$	—	140.8	ns
			Wide	$2.5\times T_C+217$	—	237.8	ns
158	Last SCK sampling edge to $\overline{HREQ}$ output not deasserted (CPHA = 1)	Slave	Bypassed	$2.5\times T_C+30$	50.8	—	ns
			Narrow	$2.5\times T_C+80$	100.8	—	ns
			Wide	$2.5\times T_C+136$	156.8	—	ns
159	$\overline{SS}$ deassertion to $\overline{HREQ}$ output not deasserted (CPHA = 0)	Slave	—	$2.5\times T_C+30$	50.8	—	ns
160	$\overline{SS}$ deassertion pulse width (CPHA = 0)	Slave	—	T_C+6	14.3	—	ns
161	$\overline{HREQ}$ in assertion to first SCK edge	Master	Bypassed	$0.5 \times t_{SPICC} + 2.5\times T_C+43$	111.8	—	ns
			Narrow	$0.5 \times t_{SPICC} + 2.5\times T_C+43$	164.8	—	ns
			Wide	$0.5 \times t_{SPICC} + 2.5\times T_C+43$	200.3	—	ns
162	$\overline{HREQ}$ in deassertion to last SCK sampling edge ($\overline{HREQ}$ in set-up time) (CPHA = 1)	Master	—	0	0	—	ns
163	First SCK edge to $\overline{HREQ}$ in not asserted ($\overline{HREQ}$ in hold time)	Master	—	0	0	—	ns

[1] V_{CC} = 3.16 V ± 0.16 V; T_J = –40°C to +110°C, C_L = 50 pF

[2] Periodically sampled, not 100% tested

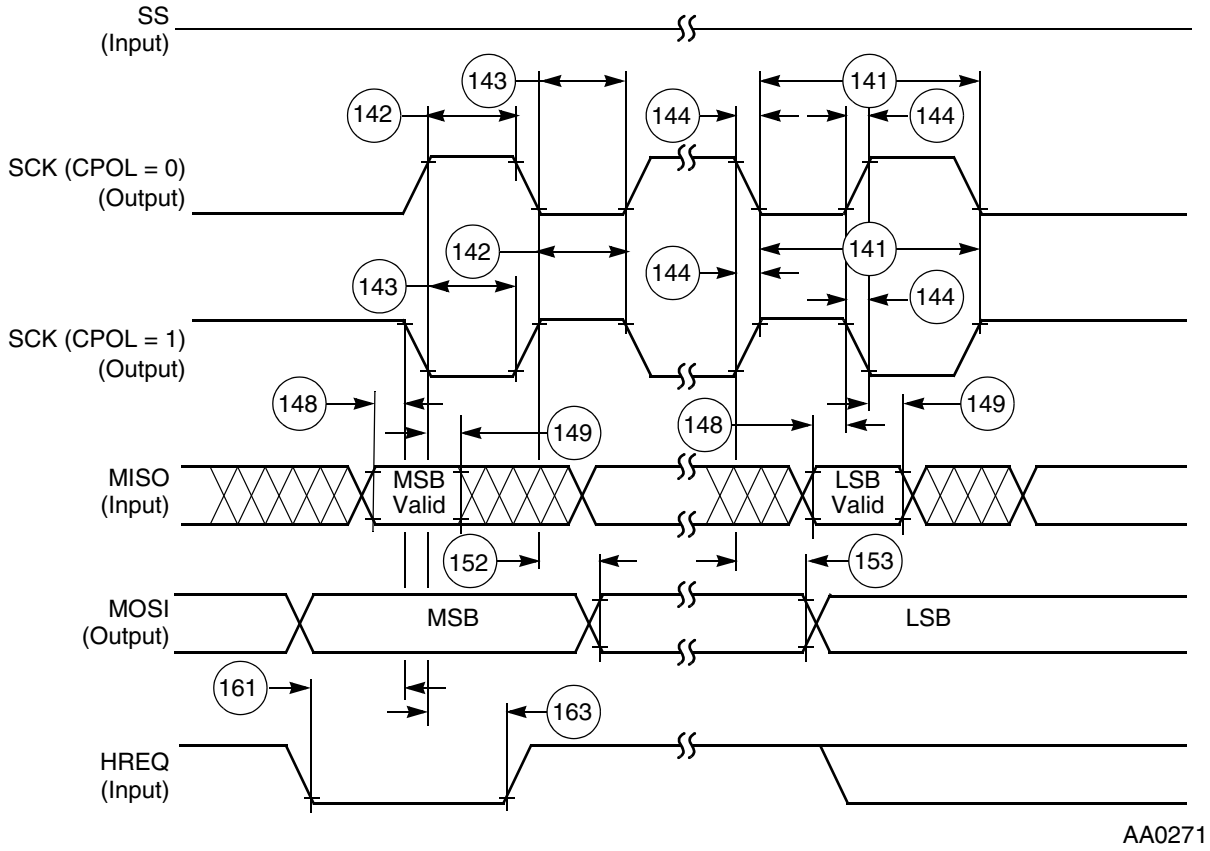


Figure 3-27 SPI Master Timing (CPHA = 0)

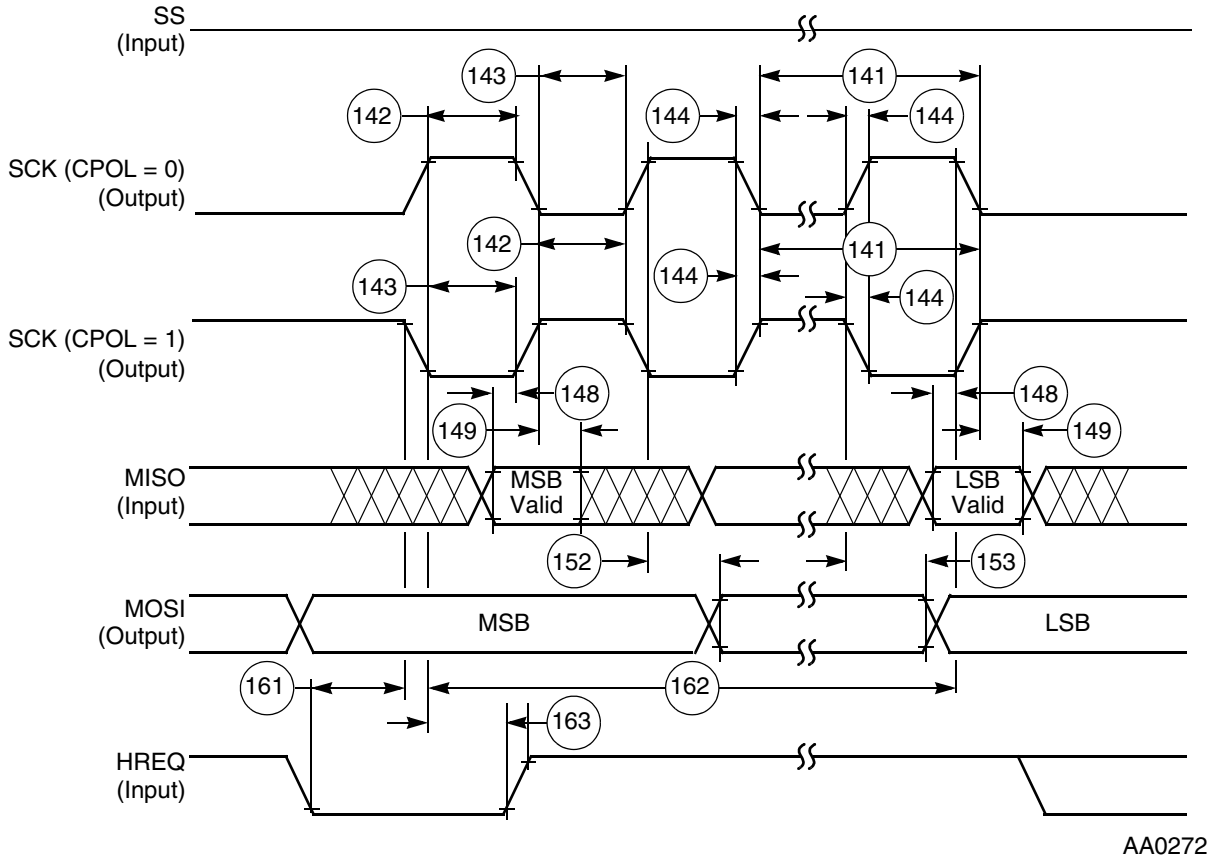


Figure 3-28 SPI Master Timing (CPHA = 1)

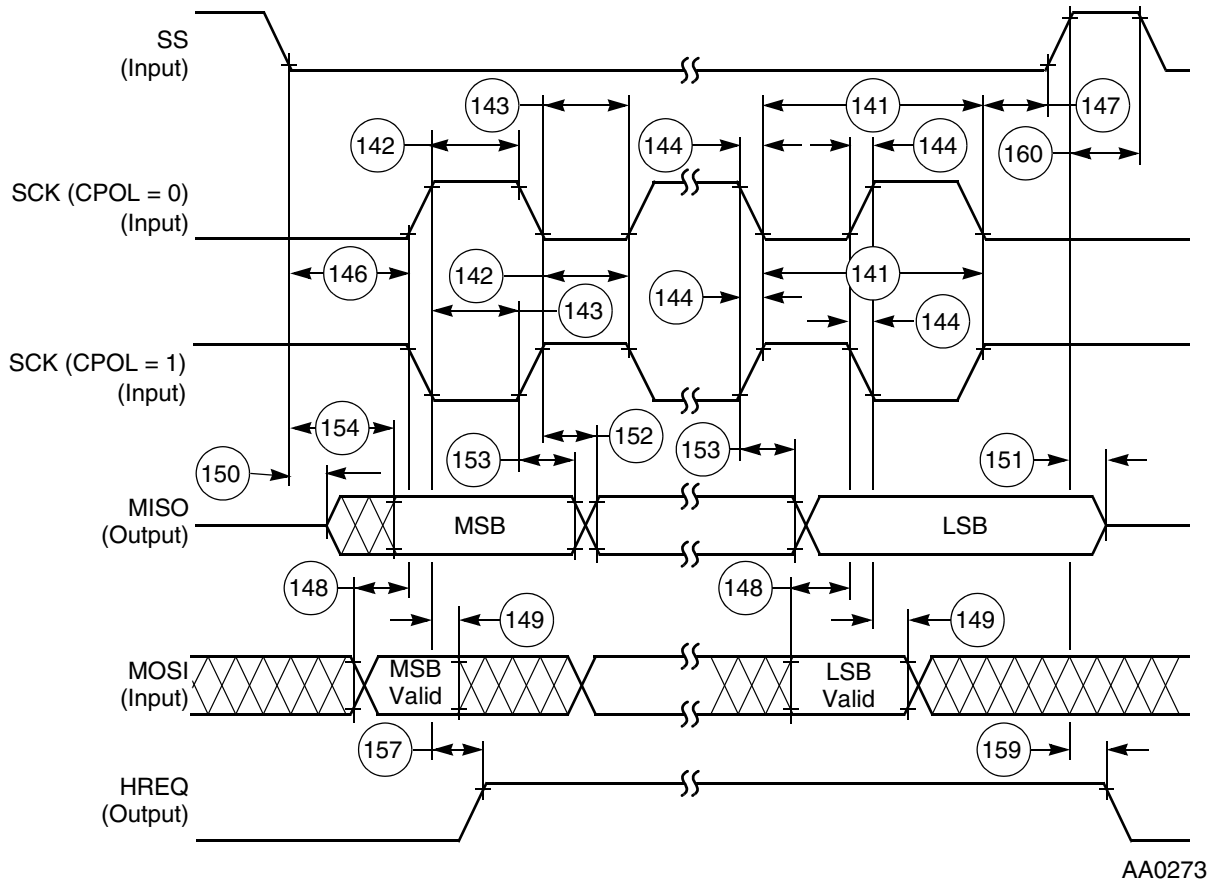


Figure 3-29 SPI Slave Timing (CPHA = 0)

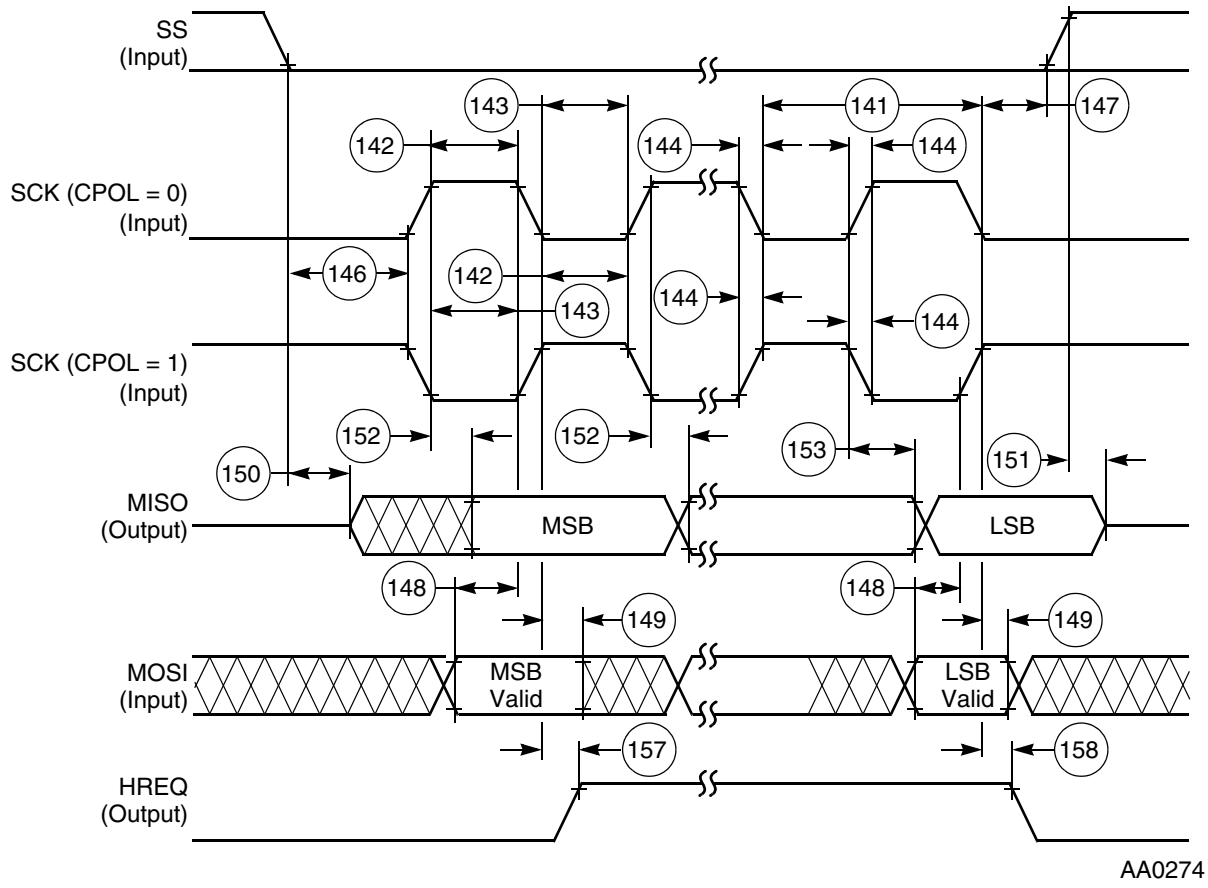


Figure 3-30 SPI Slave Timing (CPHA = 1)

3.13 Serial Host Interface (SHI) I²C Protocol Timing

Table 3-20 SHI I²C Protocol Timing

No.	Characteristics[1,2,3]	Symbol/ Expression	Standard Mode[4]		Fast Mode[5]		Unit
			Min	Max	Min	Max	
	Tolerable spike width on SCL or SDA						
	Filters bypassed	—	—	0	—	0	ns
	Narrow filters enabled		—	50	—	50	ns
	Wide filters enabled		—	100	—	100	ns
171	SCL clock frequency	F_{SCL}	—	100	—	400	kHz
171	SCL clock cycle	T_{SCL}	10	—	2.5	—	µs
172	Bus free time	T_{BUF}	4.7	—	1.3	—	µs
173	Start condition set-up time	$T_{SU;STA}$	4.7	—	0.6	—	µs
174	Start condition hold time	$T_{HD;STA}$	4.0	—	0.6	—	µs
175	SCL low period	T_{LOW}	4.7	—	1.3	—	µs
176	SCL high period	T_{HIGH}	4.0	—	1.3	—	µs
177	SCL and SDA rise time	T_R	—	1000	$20 + 0.1 \times C_b$	300	ns
178	SCL and SDA fall time	T_F	—	300	$20 + 0.1 \times C_b$	300	ns
179	Data set-up time	$T_{SU;DAT}$	250	—	100	—	ns
180	Data hold time	$T_{HD;DAT}$	0.0	—	0.0	0.9	µs
181	DSP clock frequency	F_{DSP}					MHz
	Filters bypassed		10.6	—	28.5	—	
	Narrow filters enabled		11.8	—	39.7	—	
	Wide filters enabled		13.1	—	61.0	—	
182	SCL low to data out valid	$T_{VD;DAT}$	—	3.4	—	0.9	µs
183	Stop condition set-up time	$T_{SU;STO}$	4.0	—	0.6	—	µs
184	$\overline{\text{HREQ}}$ in deassertion to last SCL edge ($\overline{\text{HREQ}}$ in set-up time)	$t_{SU;RQI}$	0.0	—	0.0	—	ns

Table 3-20 SHI I^2C Protocol Timing (continued)

No.	Characteristics[1,2,3]	Symbol/ Expression	Standard Mode[4]		Fast Mode[5]		Unit
			Min	Max	Min	Max	
186	First SCL sampling edge to $\overline{\text{HREQ}}$ output deassertion	$T_{NG;RQO}$					ns
	Filters bypassed	$2 \times T_C + 30$	—	46.7	—	46.7	
	Narrow filters enabled	$2 \times T_C + 120$	—	136.7	—	136.7	
	Wide filters enabled	$2 \times T_C + 208$	—	224.7	—	224.7	
187	Last SCL edge to $\overline{\text{HREQ}}$ output not deasserted	$T_{AS;RQO}$					ns
	Filters bypassed	$2 \times T_C + 30$	46.7	—	46.7	—	
	Narrow filters enabled	$2 \times T_C + 80$	96.7	—	96.7	—	
	Wide filters enabled	$2 \times T_C + 135$	151.6	—	151.6	—	
188	$\overline{\text{HREQ}}$ in assertion to first SCL edge	$T_{AS;RQI}$					ns
	Filters bypassed	$0.5 \times T_I 2_{CCP}$ - $0.5 \times T_C$ - 21	4440	—	1041	—	
	Narrow filters enabled		4373	—	999	—	
	Wide filters enabled		4373	—	958	—	
189	First SCL edge to $\overline{\text{HREQ}}$ in not asserted ($\overline{\text{HREQ}}$ in hold time)	$t_{HO;RQI}$	0.0	—	0.0	—	ns

1 V_{CC} = 3.16 V ± 0.16 V; T_J = –40°C to +110°C
2 Pull-up resistor: R_P (min) = 1.5 kOhm
3 Capacitive load: C_b (max) = 400 pF
4 It is recommended to enable the wide filters when operating in the I^2C Standard Mode.
5 It is recommended to enable the narrow filters when operating in the I^2C Fast Mode.

3.13.1 Programming the Serial Clock

The programmed serial clock cycle, T_{I^2CCP}, is specified by the value of the HDM[7:0] and HRS bits of the HCKR (SHI clock control register).

The expression for T_{I^2CCP} is

$$T_{I^2CCP} = [T_C \times 2 \times (HDM[7:0] + 1) \times (7 \times (1 - HRS) + 1)]$$

where

HRS is the prescaler rate select bit. When HRS is cleared, the fixed divide-by-eight prescaler is operational. When HRS is set, the prescaler is bypassed.

HDM[7:0] are the divider modulus select bits. A divide ratio from 1 to 256 (HDM[7:0] = $00 to $FF) may be selected.

In I^2C mode, the user may select a value for the programmed serial clock cycle from

$$6 \times T_C \quad \text{if HDM[7:0] = \$02 and HRS = 1}$$

to

$$4096 \times T_C \quad \text{if HDM[7:0] = \$FF and HRS = 0}$$

The programmed serial clock cycle (T_{I^2CCP}), SCL rise time (T_R), and the filters selected should be chosen in order to achieve the desired SCL serial clock cycle (T_{SCL}), as shown in Table 3-21.

Table 3-21 SCL Serial Clock Cycle (T_{SCL}) generated as Master

Filters bypassed	$T_{I^2CCP} + 2.5 \times T_C + 45ns + T_R$
Narrow filters enabled	$T_{I^2CCP} + 2.5 \times T_C + 135ns + T_R$
Wide filters enabled	$T_{I^2CCP} + 2.5 \times T_C + 223ns + T_R$

EXAMPLE:

For DSP clock frequency of 120 MHz (i.e. T_C = 8.33ns), operating in a standard mode I^2C environment (F_{SCL} = 100 kHz (i.e. T_{SCL} = 10µs), T_R = 1000ns), with wide filters enabled:

$$T_{I^2CCP} = 10\mu s - 2.5 \times 8.33ns - 223ns - 1000ns = 8756ns$$

Choosing HRS = 0 gives

$$HDM[7:0] = 8756ns/(2 \times 8.33ns \times 8) - 1 = 64.67$$

Thus the HDM[7:0] value should be programmed to $41 (=65).

The resulting T_{I^2CCP} will be:

$$T_{I^2CCP} = [T_C \times 2 \times (HDM[7:0] + 1) \times (7 \times (1 - HRS) + 1)]$$

$$T_{I^2CCP} = [8.33ns \times 2 \times (65 + 1) \times (7 \times (1 - 0) + 1)]$$

$$T_{I^2CCP} = [8.33ns \times 2 \times 66 \times 8] = 8796.48ns$$

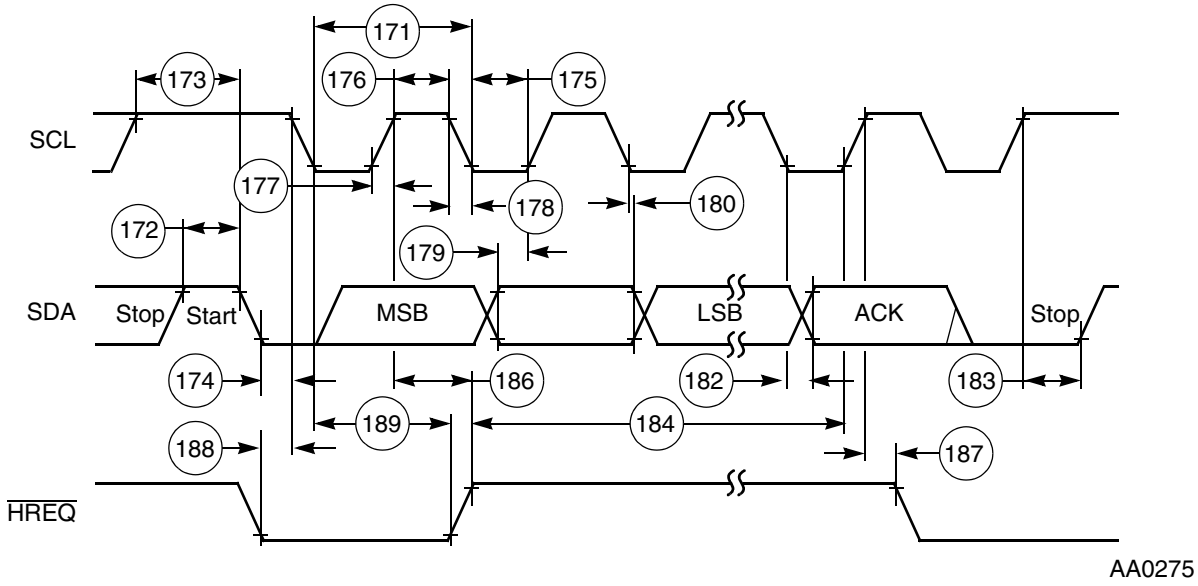


Figure 3-31 I^2C Timing

3.14 Enhanced Serial Audio Interface Timing

Table 3-22 Enhanced Serial Audio Interface Timing

No.	Characteristics[1, 2, 3]	Symbol	Expression	Min	Max	Condition[4]	Unit
430	Clock cycle[5]	t_{SSICC}	$4 \times T_C$ $3 \times T_C$ TXC:max[3*tc; t454]	33.3 25.0 27.2	— — —	i ck x ck x ck	ns
431	Clock high period • For internal clock • For external clock	—	 $2 \times T_C - 10.0$ $1.5 \times T_C$	 6.7 12.5	 — —		ns
432	Clock low period • For internal clock • For external clock	—	 $2 \times T_C - 10.0$ $1.5 \times T_C$	 6.7 12.5	 — —		ns
433	RXC rising edge to FSR out (bl) high	—	—	— —	37.0 22.0	x ck i ck a	ns
434	RXC rising edge to FSR out (bl) low	—	—	— —	37.0 22.0	x ck i ck a	ns
435	RXC rising edge to FSR out (wr) high[6]	—	—	— —	39.0 24.0	x ck i ck a	ns
436	RXC rising edge to FSR out (wr) low[6]	—	—	— —	39.0 24.0	x ck i ck a	ns
437	RXC rising edge to FSR out (wl) high	—	—	— —	36.0 21.0	x ck i ck a	ns
438	RXC rising edge to FSR out (wl) low	—	—	— —	37.0 22.0	x ck i ck a	ns
439	Data in setup time before RXC (SCK in synchronous mode) falling edge	—	—	0.0 19.0	— —	x ck i ck	ns
440	Data in hold time after RXC falling edge	—	—	5.0 3.0	— —	x ck i ck	ns
441	FSR input (bl, wr) high before RXC falling edge[6]	—	—	23.0 1.0	— —	x ck i ck a	ns
442	FSR input (wl) high before RXC falling edge	—	—	1.0 23.0	— —	x ck i ck a	ns
443	FSR input hold time after RXC falling edge	—	—	3.0 0.0	— —	x ck i ck a	ns

Table 3-22 Enhanced Serial Audio Interface Timing (continued)

No.	Characteristics[1, 2, 3]	Symbol	Expression	Min	Max	Condition[4]	Unit
444	Flags input setup before RXC falling edge	—	—	0.0 19.0	— —	x ck i ck s	ns
445	Flags input hold time after RXC falling edge	—	—	6.0 0.0	— —	x ck i ck s	ns
446	TXC rising edge to FST out (bl) high	—	—	— —	29.0 15.0	x ck i ck	ns
447	TXC rising edge to FST out (bl) low	—	—	— —	31.0 17.0	x ck i ck	ns
448	TXC rising edge to FST out (wr) high[6]	—	—	— —	31.0 17.0	x ck i ck	ns
449	TXC rising edge to FST out (wr) low[6]	—	—	— —	33.0 19.0	x ck i ck	ns
450	TXC rising edge to FST out (wl) high	—	—	— —	30.0 16.0	x ck i ck	ns
451	TXC rising edge to FST out (wl) low	—	—	— —	31.0 17.0	x ck i ck	ns
452	TXC rising edge to data out enable from high impedance	—	—	— —	31.0 17.0	x ck i ck	ns
453	TXC rising edge to transmitter #0 drive enable assertion	—	—	— —	34.0 20.0	x ck i ck	ns
454	TXC rising edge to data out valid	—	$23 + 0.5 \times T_C$ 21.0	— —	27.2 21.0	x ck i ck	ns
455	TXC rising edge to data out high impedance[7]	—	—	— —	31.0 16.0	x ck i ck	ns
456	TXC rising edge to transmitter #0 drive enable deassertion[7]	—	—	— —	34.0 20.0	x ck i ck	ns
457	FST input (bl, wr) setup time before TXC falling edge[6]	—	—	2.0 21.0	— —	x ck i ck	ns
458	FST input (wl) to data out enable from high impedance	—	—	—	27.0	—	ns
459	FST input (wl) to transmitter #0 drive enable assertion	—	—	—	31.0	—	ns

Table 3-22 Enhanced Serial Audio Interface Timing (continued)

No.	Characteristics[1, 2, 3]	Symbol	Expression	Min	Max	Condition[4]	Unit
460	FST input (wl) setup time before TXC falling edge	—	—	2.0 21.0	— —	x ck i ck	ns
461	FST input hold time after TXC falling edge	—	—	4.0 0.0	— —	x ck i ck	ns
462	Flag output valid after TXC rising edge	—	—	— —	32.0 18.0	x ck i ck	ns
463	HCKR/HCKT clock cycle	—	—	40.0	—		ns
464	HCKT input rising edge to TXC output	—	—	—	27.5		ns
465	HCKR input rising edge to RXC output	—	—	—	27.5		ns

1 V_{CC} = 3.16 V ± 0.16 V; T_J = –40°C to +110°C, C_L = 50 pF

2 i ck = internal clock
x ck = external clock
i ck a = internal clock, asynchronous mode
(asynchronous implies that TXC and RXC are two different clocks)
i ck s = internal clock, synchronous mode
(synchronous implies that TXC and RXC are the same clock)

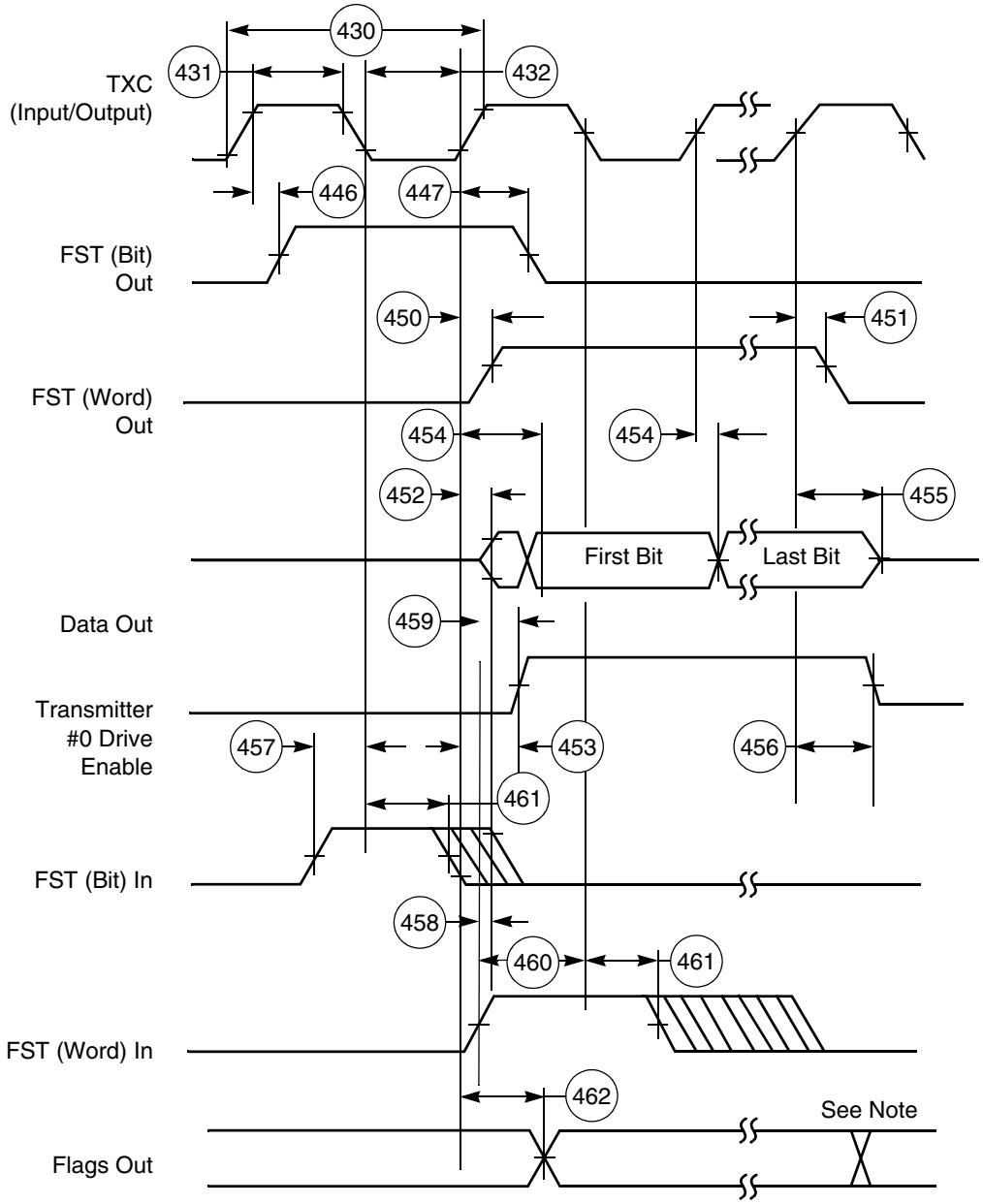
3 bl = bit length
wl = word length
wr = word length relative

4 TXC(SCKT pin) = transmit clock
RXC(SCKR pin) = receive clock
FST(FST pin) = transmit frame sync
FSR(FSR pin) = receive frame sync
HCKT(HCKT pin) = transmit high frequency clock
HCKR(HCKR pin) = receive high frequency clock

5 For the internal clock, the external clock cycle is defined by Icyc and the ESAI control register.

6 The word-relative frame sync signal waveform relative to the clock operates in the same manner as the bit-length frame sync signal waveform, but spreads from one serial clock before first bit clock (same as bit length frame sync signal), until the one before last bit clock of the first word in frame.

7 Periodically sampled and not 100% tested



Notes In network mode, output flag transitions can occur at the start of each time slot within the frame. In normal mode, the output flag state is asserted for the entire frame period.

AA0490

Figure 3-32 ESAI Transmitter Timing

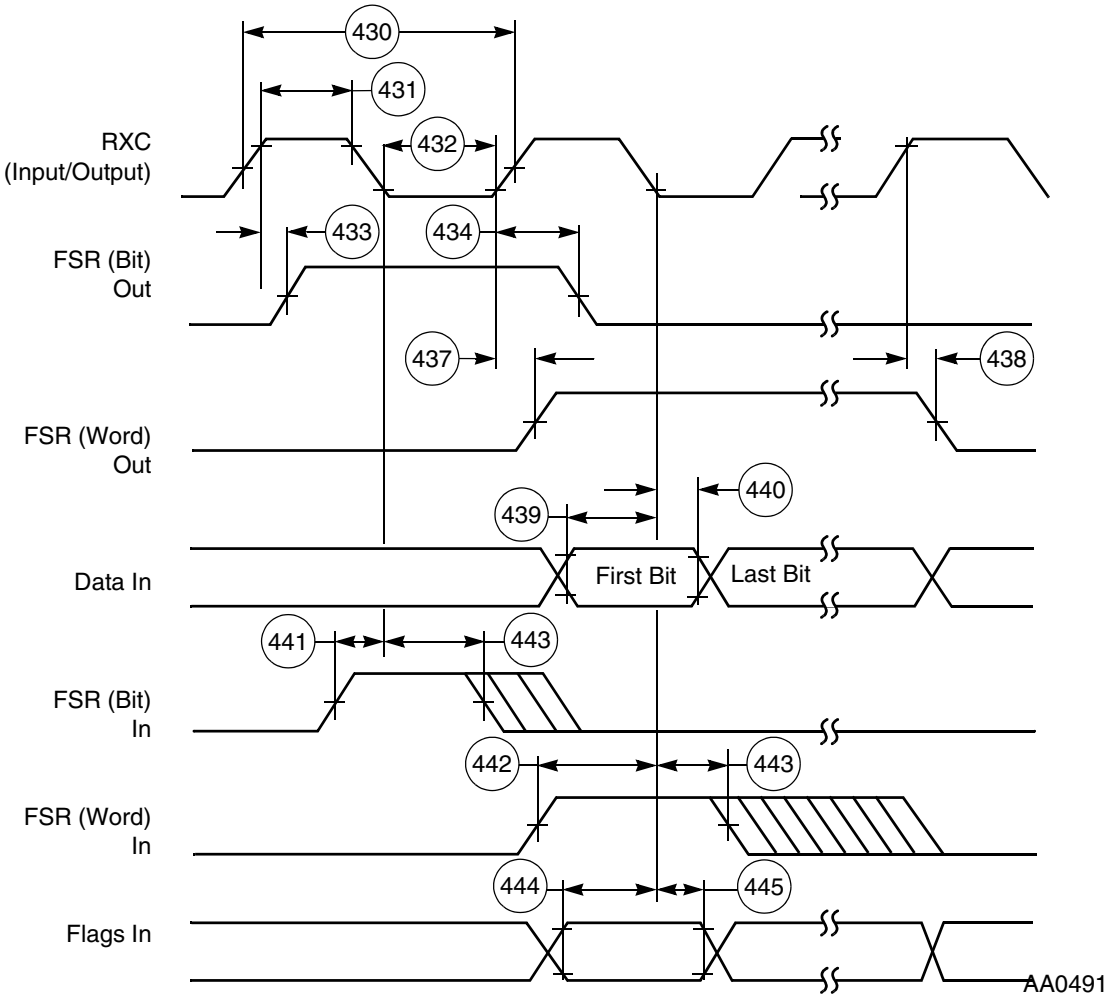


Figure 3-33 ESAI Receiver Timing

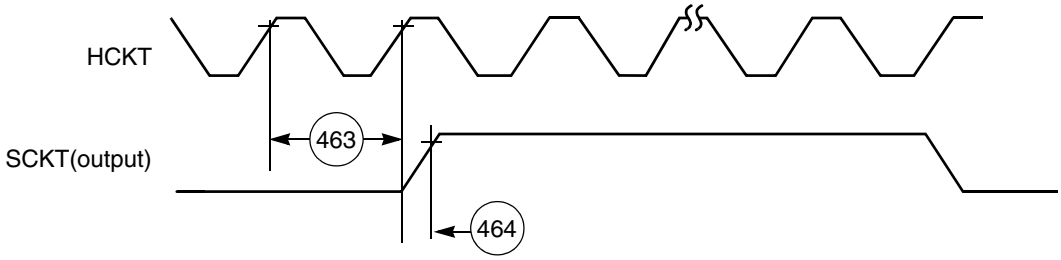


Figure 3-34 ESAI HCKT Timing

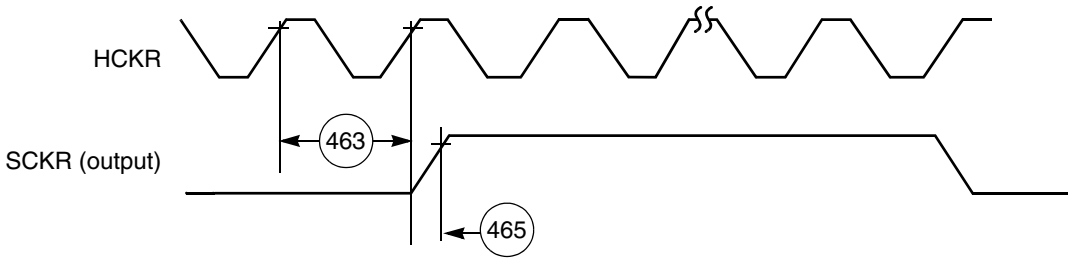


Figure 3-35 ESAI HCKR Timing

3.15 Digital Audio Transmitter Timing

Table 3-23 Digital Audio Transmitter Timing

No.	Characteristic	Expression	120 MHz		Unit
			Min	Max	
	ACI frequency (see note)	$1 / (2 \times T_C)$	—	60	MHz
220	ACI period	$2 \times T_C$	16.7	—	ns
221	ACI high duration	$0.5 \times T_C$	4.2	—	ns
222	ACI low duration	$0.5 \times T_C$	4.2	—	ns
223	ACI rising edge to ADO valid	$1.5 \times T_C$	—	12.5	ns
Note: In order to assure proper operation of the DAX, the ACI frequency should be less than 1/2 of the DSP56366 internal clock frequency. For example, if the DSP56366 is running at 120 MHz internally, the ACI frequency should be less than 60 MHz.					

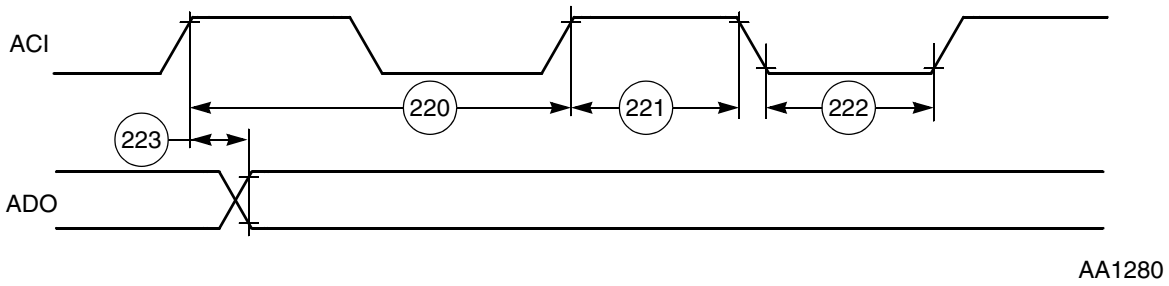


Figure 3-36 Digital Audio Transmitter Timing

3.16 Timer Timing

Table 3-24 Timer Timing

No.	Characteristics	Expression	120 MHz		Unit
			Min	Max	
480	TIO Low	$2 \times T_C + 2.0$	18.7	—	ns
481	TIO High	$2 \times T_C + 2.0$	18.7	—	ns
Note: V_{CC} = 3.3 V ± 0.16 V; T_J = –40°C to +110°C, C_L = 50 pF					

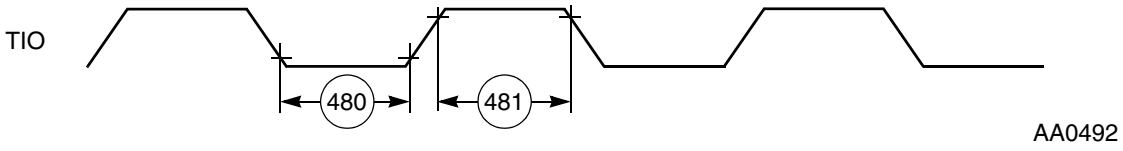


Figure 3-37 TIO Timer Event Input Restrictions

3.17 GPIO Timing

Table 3-25 GPIO Timing

No.	Characteristics[1]	Expression	Min	Max	Unit
490[2]	EXTAL edge to GPIO out valid (GPIO out delay time)		—	32.8	ns
491	EXTAL edge to GPIO out not valid (GPIO out hold time)		4.8	—	ns
492	GPIO In valid to EXTAL edge (GPIO in set-up time)		10.2	—	ns
493	EXTAL edge to GPIO in not valid (GPIO in hold time)		1.8	—	ns
494[2]	Fetch to EXTAL edge before GPIO change	$6.75 \times T_C$-1.8	54.5	—	ns
495	GPIO out rise time	—	—	13	ns
496	GPIO out fall time	—	—	13	ns

1 V_{CC} = 3.3 V ± 0.16 V; T_J = –40°C to +110°C, C_L = 50 pF
2 Valid only when PLL enabled with multiplication factor equal to one.

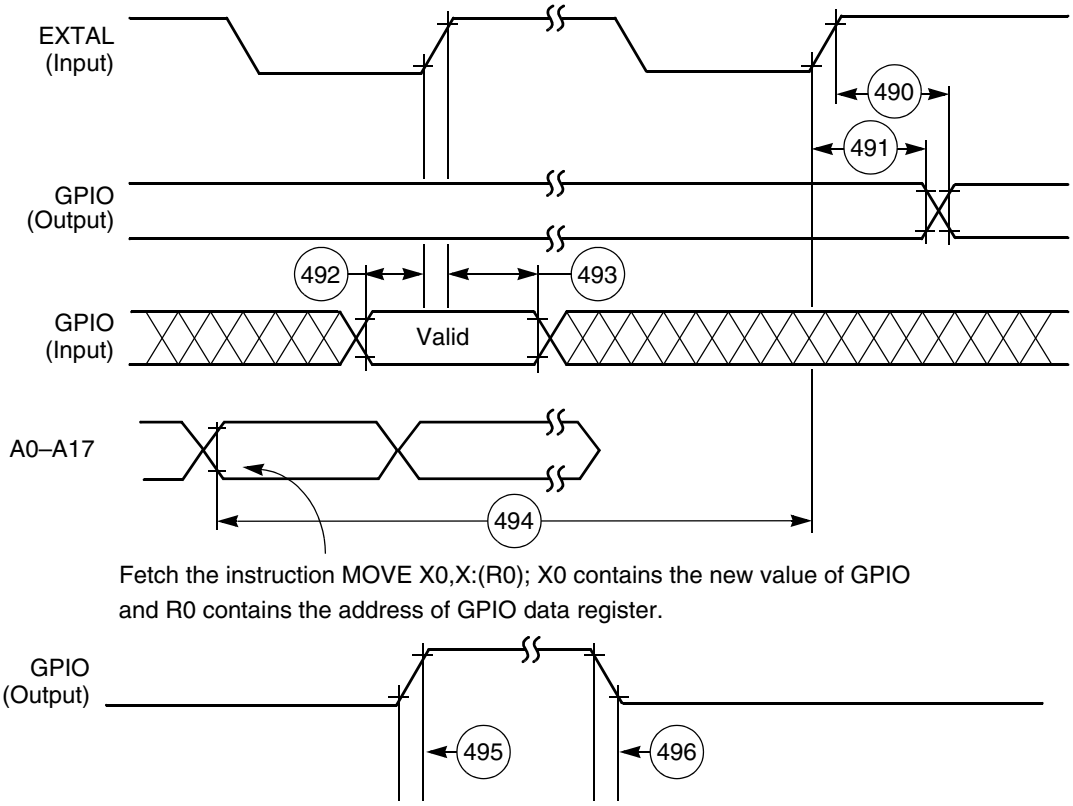


Figure 3-38 GPIO Timing

3.18 JTAG Timing

Table 3-26 JTAG Timing[1, 2]

No.	Characteristics	All frequencies		Unit
		Min	Max	
500	TCK frequency of operation ($1/(T_C \times 3)$; maximum 22 MHz)	0.0	22.0	MHz
501	TCK cycle time in Crystal mode	45.0	—	ns
502	TCK clock pulse width measured at 1.5 V	20.0	—	ns
503	TCK rise and fall times	0.0	3.0	ns
504	Boundary scan input data setup time	5.0	—	ns
505	Boundary scan input data hold time	24.0	—	ns
506	TCK low to output data valid	0.0	40.0	ns
507	TCK low to output high impedance	0.0	40.0	ns
508	TMS, TDI data setup time	5.0	—	ns

Table 3-26 JTAG Timing[1, 2] (continued)

No.	Characteristics	All frequencies		Unit
		Min	Max	
509	TMS, TDI data hold time	25.0	—	ns
510	TCK low to TDO data valid	0.0	44.0	ns
511	TCK low to TDO high impedance	0.0	44.0	ns
Notes: 1. 4.				

1 V_{CC} = 3.3 V ± 0.16 V; T_J = –40°C to +110°C, C_L = 50 pF

2 All timings apply to OnCE module data transfers because it uses the JTAG port as an interface.

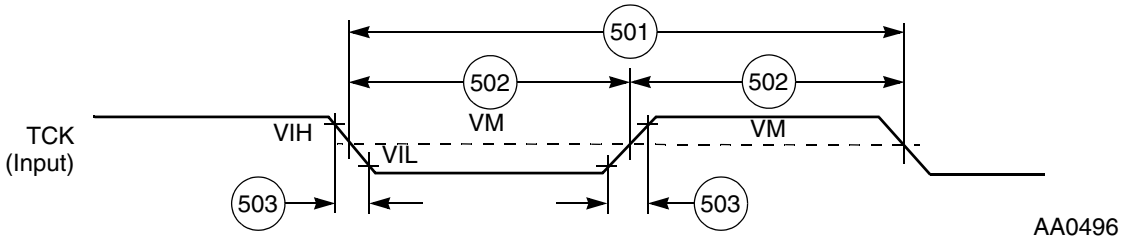


Figure 3-39 Test Clock Input Timing Diagram

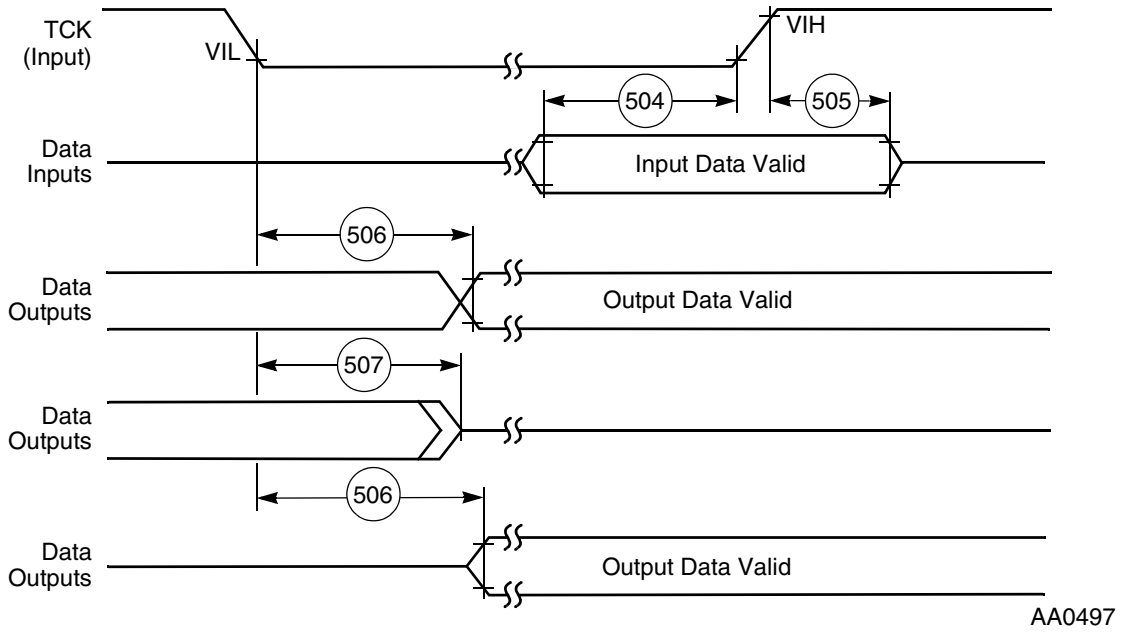


Figure 3-40 Boundary Scan (JTAG) Timing Diagram

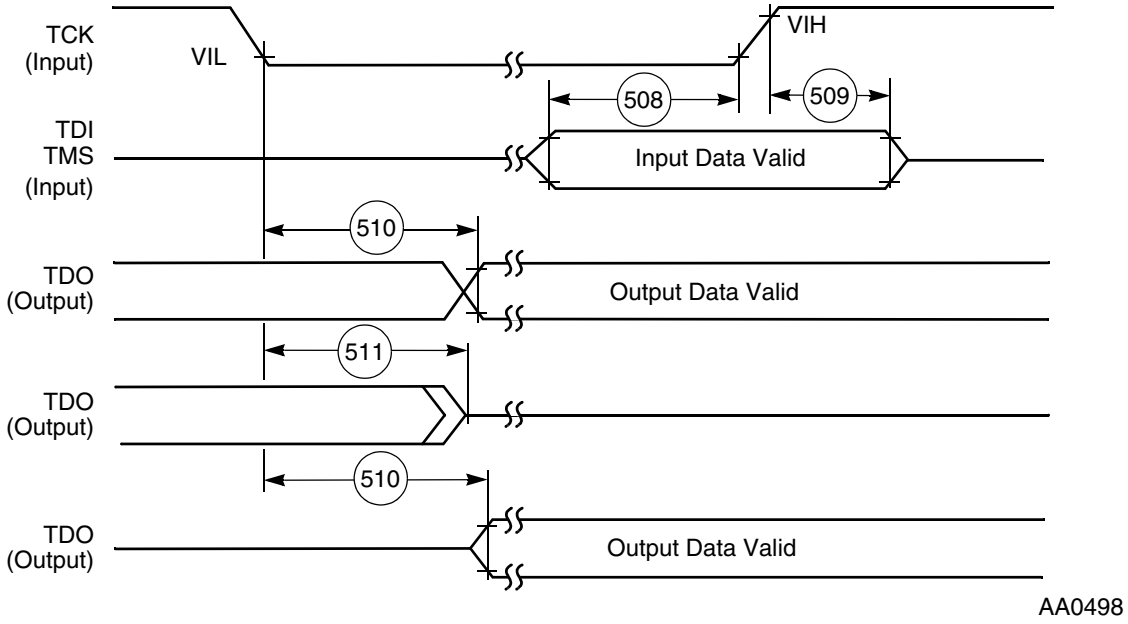


Figure 3-41 Test Access Port Timing Diagram

NOTES

4 Packaging

4.1 Pin-out and Package Information

This section provides information about the available package for this product, including diagrams of the package pinouts and tables describing how the signals described in Section 2, “Signal/Connection Descriptions” 1 are allocated for the package. The DSP56366 is available in a 144-pin LQFP package. Table 4-1 and Table 4-2 show the pin/name assignments for the packages.

4.1.1 LQFP Package Description

Top view of the 144-pin LQFP package is shown in Figure 4-1 with its pin-outs. The package drawing is shown in Figure 4-2.

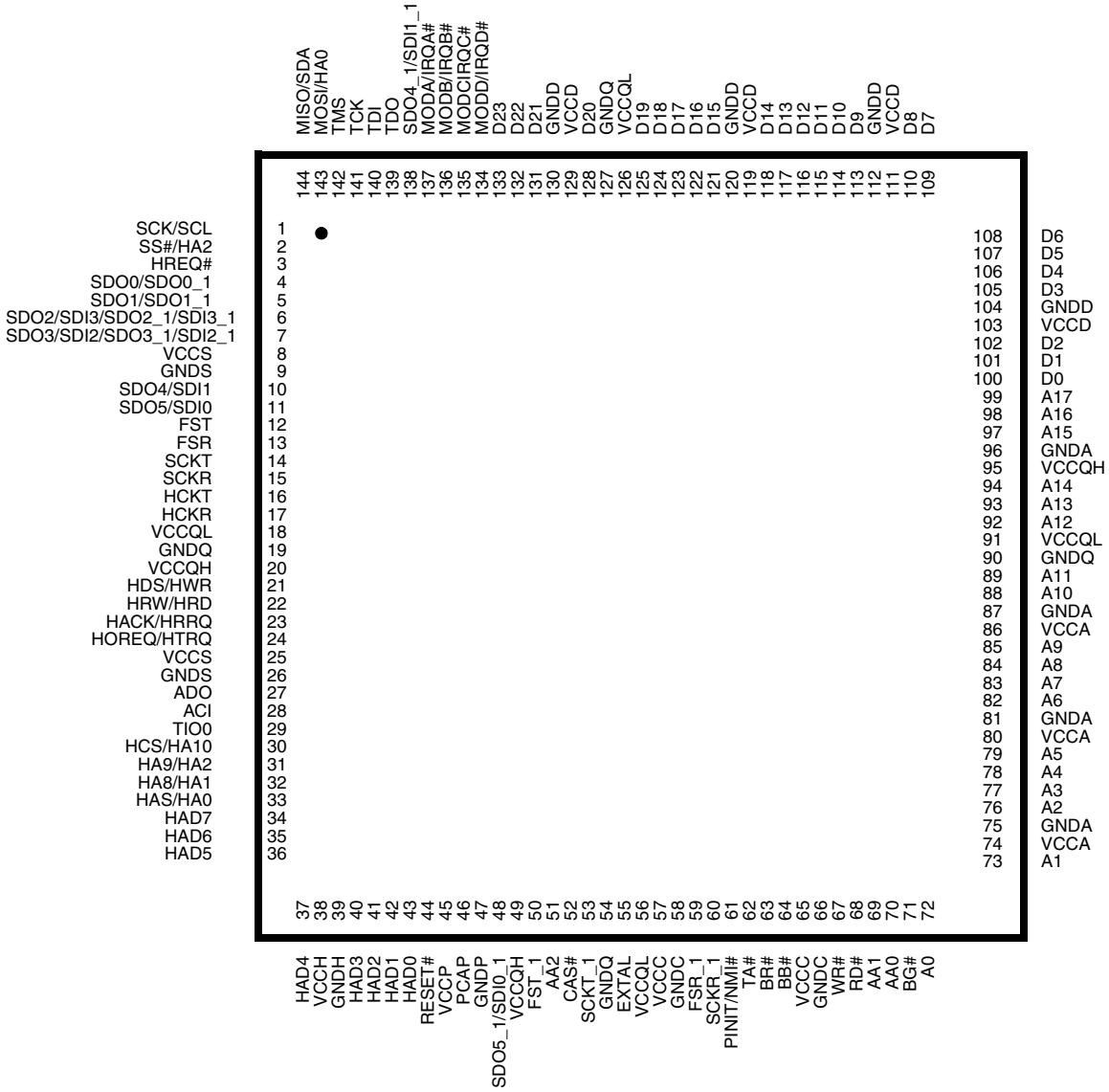


Figure 4-1 144-pin package

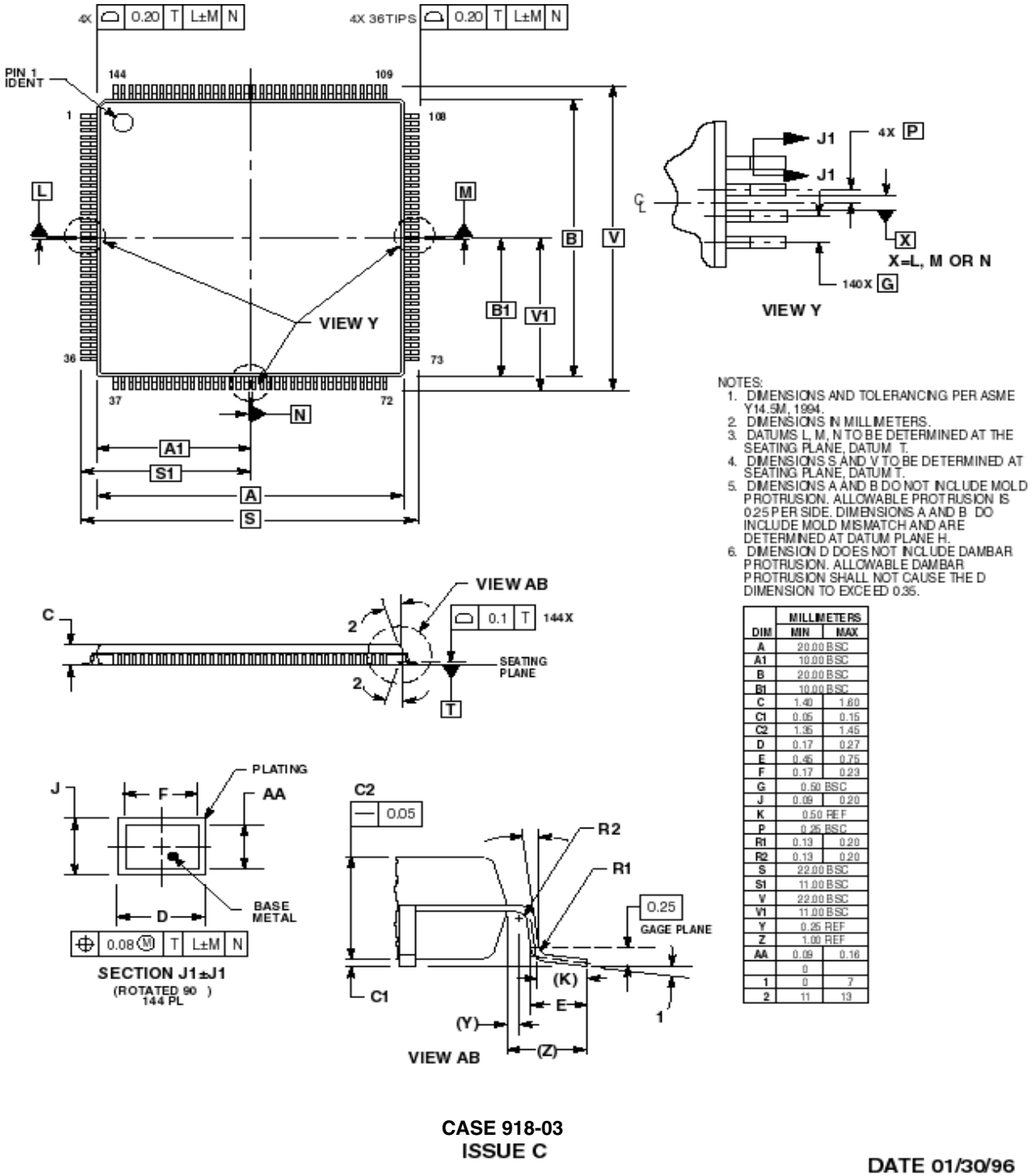
Table 4-1 Signal Identification by Name

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
A0	72	D9	113	GNDS	9	SDO0/SDO0_1	4
A1	73	D10	114	GNDS	26	SDO1/SDO1_1	5
A2	76	D11	115	HA8/HA1	32	SDO2/SDI3/SDO2_1/SDI3_1	6
A3	77	D12	116	HA9/HA2	31	SDO3/SDI2/SDO3_1/SDI2_1	7
A4	78	D13	117	HACK/HRRQ	23	SDO4/SDI1	10
A5	79	D14	118	HAD0	43	SDO4_1/SDI1_1	138
A6	82	D15	121	HAD1	42	SDO5/SDI0	11
A7	83	D16	122	HAD2	41	SDO5_1/SDI0_1	48
A8	84	D17	123	HAD3	40	SS#/HA2	2
A9	85	D18	124	HAD4	37	TA#	62
A10	88	D19	125	HAD5	36	TCK	141
A11	89	D20	128	HAD6	35	TDI	140
A12	92	D21	131	HAD7	34	TDO	139
A13	93	D22	132	HAS/HA0	33	TIO0	29
A14	94	D23	133	HCKR	17	TMS	142
A15	97	EXTAL	55	HCKT	16	VCCA	74
A16	98	FSR	13	HCS/HA10	30	VCCA	80
A17	99	FSR_1	59	HDS/HWR	21	VCCA	86
AA0	70	FST	12	HOREQ/HTRQ	24	VCCC	57
AA1	69	FST_1	50	HREQ#	3	VCCC	65
AA2	51	GNDA	75	HRW/HRD	22	VCCD	103
ACI	28	GNDA	81	MODA/IRQA#	137	VCCD	111
ADO	27	GNDA	87	MODB/IRQB#	136	VCCD	119
BB#	64	GNDA	96	MODC/IRQC#	135	VCCD	129
BG#	71	GNDC	58	MODD/IRQD#	134	VCCH	38
BR#	63	GNDC	66	MISO/SDA	144	VCCQH	20
CAS#	52	GNDD	104	MOSI/HA0	143	VCCQH	95
D0	100	GNDD	112	PCAP	46	VCCQH	49
D1	101	GNDD	120	PINIT/NMI#	61	VCCQL	18
D2	102	GNDD	130	RD#	68	VCCQL	56
D3	105	GNDH	39	RESET#	44	VCCQL	91
D4	106	GNDP	47	SCK/SCL	1	VCCQL	126
D5	107	GNDQ	19	SCKR	15	VCCP	45
D6	108	GNDQ	54	SCKR_1	60	VCCS	8
D7	109	GNDQ	90	SCKT	14	VCCS	25
D8	110	GNDQ	127	SCKT_1	53	WR#	67

Table 4-2 Signal Identification by Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	SCK/SCL	37	HAD4	73	A1	109	D7
2	SS#/HA2	38	VCCH	74	VCCA	110	D8
3	HREQ#	39	GNDH	75	GNDA	111	VCCD
4	SDO0/SDO0_1	40	HAD3	76	A2	112	GNDD
5	SDO1/SDO1_1	41	HAD2	77	A3	113	D9
6	SDO2/SDI3/SDO2_1/SDI3_1	42	HAD1	78	A4	114	D10
7	SDO3/SDI2/SDO3_1/SDI2_1	43	HAD0	79	A5	115	D11
8	VCCS	44	RESET#	80	VCCA	116	D12
9	GNDS	45	VCCP	81	GNDA	117	D13
10	SDO4/SDI1	46	PCAP	82	A6	118	D14
11	SDO5/SDI0	47	GND	83	A7	119	VCCD
12	FST	48	SDO5_1/SDI0_1	84	A8	120	GNDD
13	FSR	49	VCCQH	85	A9	121	D15
14	SCKT	50	FST_1	86	VCCA	122	D16
15	SCKR	51	AA2	87	GNDA	123	D17
16	HCKT	52	CAS#	88	A10	124	D18
17	HCKR	53	SCKT_1	89	A11	125	D19
18	VCCQL	54	GNDQ	90	GNDQ	126	VCCQL
19	GNDQ	55	EXTAL	91	VCCQL	127	GNDQ
20	VCCQH	56	VCCQL	92	A12	128	D20
21	HDS/HWR	57	VCCC	93	A13	129	VCCD
22	HRW/HRD	58	GNDC	94	A14	130	GNDD
23	HACK/HRRQ	59	FSR_1	95	VCCQH	131	D21
24	HOREQ/HTRQ	60	SCKR_1	96	GNDA	132	D22
25	VCCS	61	PINIT/NMI#	97	A15	133	D23
26	GNDS	62	TA#	98	A16	134	MODD/IRQD#
27	ADO	63	BR#	99	A17	135	MODC/IRQC#
28	ACI	64	BB#	100	D0	136	MODB/IRQB#
29	TIO0	65	VCCC	101	D1	137	MODA/IRQA#
30	HCS/HA10	66	GNDC	102	D2	138	SDO4_1/SDI1_1
31	HA9/HA2	67	WR#	103	VCCD	139	TDO
32	HA8/HA1	68	RD#	104	GNDD	140	TDI
33	HAS/HA0	69	AA1	105	D3	141	TCK
34	HAD7	70	AA0	106	D4	142	TMS
35	HAD6	71	BG#	107	D5	143	MOSI/HA0
36	HAD5	72	A0	108	D6	144	MISO/SDA

4.1.2 LQFP Package Mechanical Drawing



DIM	MILLIMETERS MIN	MAX
A	20.00 BSC	
A1	10.00 BSC	
B	20.00 BSC	
B1	10.00 BSC	
C	1.40	1.60
C1	0.05	0.15
C2	1.35	1.45
D	0.17	0.27
E	0.45	0.75
F	0.17	0.23
G	0.50 BSC	
J	0.09	0.20
K	0.50 REF	
P	0.25 BSC	
R1	0.13	0.20
R2	0.13	0.20
S	22.00 BSC	
S1	11.00 BSC	
V	22.00 BSC	
V1	11.00 BSC	
Y	0.25 REF	
Z	1.00 REF	
AA	0.09	0.16
	0	
1	0	7
2	11	13

CASE 918-03
ISSUE C

DATE 01/30/96

Figure 4-2 DSP56366 144-pin LQFP Package

5 Design Considerations

5.1 Thermal Design Considerations

An estimation of the chip junction temperature, T_J, in °C can be obtained from the following equation:

$$T_J = T_A + (P_D \times R_{\theta JA})$$

Where:

T_A = ambient temperature °C
R_{qJA} = package junction-to-ambient thermal resistance °C/W
P_D = power dissipation in package W

Historically, thermal resistance has been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance.

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

Where:

$R_{\theta JA}$ = package junction-to-ambient thermal resistance °C/W
$R_{\theta JC}$ = package junction-to-case thermal resistance °C/W
$R_{\theta CA}$ = package case-to-ambient thermal resistance °C/W

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board (PCB), or otherwise change the thermal dissipation capability of the area surrounding the device on a PCB. This model is most useful for ceramic packages with heat sinks; some 90% of the heat flow is dissipated through the case to the heat sink and out to the ambient environment. For ceramic packages, in situations where the heat flow is split between a path to the case and an alternate path through the PCB, analysis of the device thermal performance may need the additional modeling capability of a system level thermal simulation tool.

The thermal performance of plastic packages is more dependent on the temperature of the PCB to which the package is mounted. Again, if the estimations obtained from $R_{\theta JA}$ do not satisfactorily answer whether the thermal performance is adequate, a system level model may be appropriate.

A complicating factor is the existence of three common ways for determining the junction-to-case thermal resistance in plastic packages.

- To minimize temperature variation across the surface, the thermal resistance is measured from the junction to the outside surface of the package (case) closest to the chip mounting area when that surface has a proper heat sink.

- To define a value approximately equal to a junction-to-board thermal resistance, the thermal resistance is measured from the junction to where the leads are attached to the case.
- If the temperature of the package case (T_T) is determined by a thermocouple, the thermal resistance is computed using the value obtained by the equation $(T_J - T_T)/P_D$.

As noted above, the junction-to-case thermal resistances quoted in this data sheet are determined using the first definition. From a practical standpoint, that value is also suitable for determining the junction temperature from a case thermocouple reading in forced convection environments. In natural convection, using the junction-to-case thermal resistance to estimate junction temperature from a thermocouple reading on the case of the package will estimate a junction temperature slightly hotter than actual temperature. Hence, the new thermal metric, thermal characterization parameter or Ψ_{JT}, has been defined to be $(T_J - T_T)/P_D$. This value gives a better estimate of the junction temperature in natural convection when using the surface temperature of the package. Remember that surface temperature readings of packages are subject to significant errors caused by inadequate attachment of the sensor to the surface and to errors caused by heat loss to the sensor. The recommended technique is to attach a 40-gauge thermocouple wire and bead to the top center of the package with thermally conductive epoxy.

5.2 Electrical Design Considerations

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields. However, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). The suggested value for a pullup or pulldown resistor is 10 kOhm.

Use the following list of recommendations to assure correct DSP operation:

- Provide a low-impedance path from the board power supply to each V_{CC} pin on the DSP and from the board ground to each GND pin.
- Use at least six 0.01–0.1 µF bypass capacitors positioned as close as possible to the four sides of the package to connect the V_{CC} power source to GND.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{CC} and GND pins are less than 1.2 cm (0.5 inch) per capacitor lead.
- Use at least a four-layer PCB with two inner layers for V_{CC} and GND.
- Because the DSP output signals have fast rise and fall times, PCB trace lengths should be minimal. This recommendation particularly applies to the address and data buses as well as the $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, $\overline{\text{TA}}$ and $\overline{\text{BG}}$ pins. Maximum PCB trace lengths on the order of 15 cm (6 inches) are recommended.
- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{CC} and GND circuits.
- All inputs must be terminated (i.e., not allowed to float) using CMOS levels, except for the three pins with internal pull-up resistors (TMS, $\overline{\text{TDI}}$, TCK).

- Take special care to minimize noise levels on the V_{CCP} and GND_P pins.
- If multiple DSP56366 devices are on the same board, check for cross-talk or excessive spikes on the supplies due to synchronous operation of the devices.
- $\overline{\text{RESET}}$ must be asserted when the chip is powered up. A stable EXTAL signal must be supplied while $\overline{\text{RESET}}$ is being asserted.
- At power-up, ensure that the voltage difference between the 5 V tolerant pins and the chip V_{CC} never exceeds 3.95 V.

5.3 Power Consumption Considerations

Power dissipation is a key issue in portable DSP applications. Some of the factors which affect current consumption are described in this section. Most of the current consumed by CMOS devices is alternating current (ac), which is charging and discharging the capacitances of the pins and internal nodes.

Current consumption is described by the following formula:

$$I = C \times V \times f$$

where:

C = node/pin capacitance
V = voltage swing
f = frequency of node/pin toggle

Example 1. Current Consumption

For a Port A address pin loaded with 50 pF capacitance, operating at 3.3 V, and with a 120 MHz clock, toggling at its maximum possible rate (60 MHz), the current consumption is

$$I = 50 \times 10^{-12} \times 3.3 \times 60 \times 10^{6} = 9.9\text{mA}$$

The maximum internal current (I_{CCI}max) value reflects the typical possible switching of the internal buses on best-case operation conditions, which is not necessarily a real application case. The typical internal current (I_{CCItyp}) value reflects the average switching of the internal buses on typical operating conditions.

For applications that require very low current consumption, do the following:

- Set the EBD bit when not accessing external memory.
- Minimize external memory accesses and use internal memory accesses.
- Minimize the number of pins that are switching.
- Minimize the capacitive load on the pins.
- Connect the unused inputs to pull-up or pull-down resistors.
- Disable unused peripherals.

One way to evaluate power consumption is to use a current per MIPS measurement methodology to minimize specific board effects (i.e., to compensate for measured board current not caused by the DSP). A benchmark power consumption test algorithm is listed in **Appendix A**. Use the test algorithm, specific test current measurements, and the following equation to derive the current per MIPS value.

$$I/MIPS = I/MHz = (I_{typF2} - I_{typF1})/(F2 = F1)$$

where:

I_{typF2} = current at F2
I_{typF1} = current at F1
F2 = high frequency (any specified operating frequency)
F1 = low frequency (any specified operating frequency lower than F2)

NOTE

F1 should be significantly less than F2. For example, F2 could be 66 MHz and F1 could be 33 MHz. The degree of difference between F1 and F2 determines the amount of precision with which the current rating can be determined for an application.

5.4 PLL Performance Issues

The following explanations should be considered as general observations on expected PLL behavior. There is no testing that verifies these exact numbers. These observations were measured on a limited number of parts and were not verified over the entire temperature and voltage ranges.

5.4.1 Phase Jitter Performance

The phase jitter of the PLL is defined as the variations in the skew between the falling edges of EXTAL and the internal DSP clock for a given device in specific temperature, voltage, input frequency and MF. These variations are a result of the PLL locking mechanism. For input frequencies greater than 15 MHz and MF ≤ 4, this jitter is less than ±0.6 ns; otherwise, this jitter is not guaranteed. However, for MF < 10 and input frequencies greater than 10 MHz, this jitter is less than ±2 ns.

5.4.2 Frequency Jitter Performance

The frequency jitter of the PLL is defined as the variation of the frequency of the internal DSP clock. For small MF (MF < 10) this jitter is smaller than 0.5%. For mid-range MF (10 < MF < 500) this jitter is between 0.5% and approximately 2%. For large MF (MF > 500), the frequency jitter is 2–3%.

5.4.3 Input (EXTAL) Jitter Requirements

The allowed jitter on the frequency of EXTAL is 0.5%. If the rate of change of the frequency of EXTAL is slow (i.e., it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (i.e., it does not stay at an extreme value for a long time), then the allowed jitter can be 2%. The phase and frequency jitter performance results are only valid if the input jitter is less than the prescribed values.

5.5 Host Port Considerations

Careful synchronization is required when reading multi-bit registers that are written by another asynchronous system. This synchronization is a common problem when two asynchronous systems are connected, as they are in the host interface. The following paragraphs present considerations for proper operation.

5.5.1 Host Programming Considerations

- **Unsynchronized Reading of Receive Byte Registers**—When reading the receive byte registers, receive register high (RXH), receive register middle (RXM), or receive register low (RXL), the host interface programmer should use interrupts or poll the receive register data full (RXDF) flag that indicates whether data is available. This ensures that the data in the receive byte registers will be valid.
- **Overwriting Transmit Byte Registers**—The host interface programmer should not write to the transmit byte registers, transmit register high (TXH), transmit register middle (TXM), or transmit register low (TXL), unless the transmit register data empty (TXDE) bit is set, indicating that the transmit byte registers are empty. This ensures that the transmit byte registers will transfer valid data to the host receive (HRX) register.
- **Synchronization of Status Bits from DSP to Host**—HC, $\overline{\text{HOREQ}}$, DMA, HF3, HF2, TRDY, TXDE, and RXDF status bits are set or cleared from inside the DSP and read by the host processor (refer to the user's manual for descriptions of these status bits). The host can read these status bits very quickly without regard to the clock rate used by the DSP, but the state of the bit could be changing during the read operation. This is not generally a system problem, because the bit will be read correctly in the next pass of any host polling routine.

  However, if the host asserts $\overline{\text{HEN}}$ for more than timing number 31, with a minimum cycle time of timing number 31 + 32, then these status bits are guaranteed to be stable. Exercise care when reading status bits HF3 and HF2 as an encoded pair. If the DSP changes HF3 and HF2 from 00 to 11, there is a small probability that the host could read the bits during the transition and receive 01 or 10 instead of 11. If the combination of HF3 and HF2 has significance, the host could read the wrong combination. Therefore, read the bits twice and check for consensus.
- **Overwriting the Host Vector**—The host interface programmer should change the host vector (HV) register only when the host command (HC) bit is clear. This ensures that the DSP interrupt control logic will receive a stable vector.
- **Cancelling a Pending Host Command Exception**—The host processor may elect to clear the HC bit to cancel the host command exception request at any time before it is recognized by the DSP. Because the host does not know exactly when the exception will be recognized (due to exception processing synchronization and pipeline delays), the DSP may execute the host command exception after the HC bit is cleared. For these reasons, the HV bits must not be changed at the same time that the HC bit is cleared.
- **Variance in the Host Interface Timing**—The host interface (HDI) may vary (e.g. due to the PLL lock time at reset). Therefore, a host which attempts to load (bootstrap) the DSP should first make

sure that the part has completed its HI port programming (e.g., by setting the INIT bit in ICR then polling it and waiting it to be cleared, then reading the ISR or by writing the TREQ/RREQ together with the INIT and then polling INIT, ISR, and the $\overline{\text{HOREQ}}$ pin).

5.5.2 DSP Programming Considerations

- **Synchronization of Status Bits from Host to DSP**—DMA, HF1, HF0, HCP, HTDE, and HRDF status bits are set or cleared by the host processor side of the interface. These bits are individually synchronized to the DSP clock. (Refer to the user's manual for descriptions of these status bits.)
- **Reading HF0 and HF1 as an Encoded Pair**—Care must be exercised when reading status bits HF0 and HF1 as an encoded pair, (i.e., the four combinations 00, 01, 10, and 11 each have significance). A very small probability exists that the DSP will read the status bits synchronized during transition. Therefore, HF0 and HF1 should be read twice and checked for consensus.

6 Ordering Information

Consult a Freescale Semiconductor, Inc. sales office or authorized distributor to determine product availability and to place an order.

For information on ordering DSP Audio products, refer to the current SG1004, DSP Selector Guide, at

http://www.freescale.com

NOTES

Appendix A Power Consumption Benchmark

The following benchmark program permits evaluation of DSP power usage in a test situation. It enables the PLL, disables the external clock, and uses repeated multiply-accumulate instructions with a set of synthetic DSP application data to emulate intensive sustained DSP operation.

```
;*****************************************************************;*********
**********************************************************

;* ;* CHECKS   Typical Power Consumption

;*****************************************************************
          page     200,55,0,0,0
          nolist

I_VEC EQU $000000  ; Interrupt vectors for program debug only
START EQU $8000    ; MAIN (external) program starting address
INT_PROG  EQU $100 ; INTERNAL program memory starting address
INT_XDAT  EQU $0   ; INTERNAL X-data memory starting address
INT_YDAT  EQU $0   ; INTERNAL Y-data memory starting address

          INCLUDE "ioequ.asm"
          INCLUDE "intequ.asm"

          list

          org      P:START
;
          movep #$0123FF,x:M_BCR; BCR: Area 3 : 1 w.s (SRAM)
; Default: 1 w.s (SRAM)
;
          movep    #$0d0000,x:M_PCTL           ; XTAL disable
                             ; PLL enable
                             ; CLKOUT disable
;
; Load the program
;
          move     #INT_PROG,r0
          move     #PROG_START,r1
          do       #(PROG_END-PROG_START),PLOAD_LOOP
          move     p:(r1)+,x0
          move     x0,p:(r0)+
          nop
PLOAD_LOOP
;
; Load the X-data
;
          move     #INT_XDAT,r0
```

```
          move      #XDAT_START,r1
          do        #(XDAT_END-XDAT_START),XLOAD_LOOP
          move      p:(r1)+,x0
          move      x0,x:(r0)+
XLOAD_LOOP
;
; Load the Y-data
;
          move      #INT_YDAT,r0
          move      #YDAT_START,r1
          do        #(YDAT_END-YDAT_START),YLOAD_LOOP
          move      p:(r1)+,x0
          move      x0,y:(r0)+
YLOAD_LOOP
;

          jmp       INT_PROG

PROG_START
          move      #$0,r0
          move      #$0,r4
          move      #$3f,m0
          move      #$3f,m4
;
          clr       a
          clr       b
          move      #$0,x0
          move      #$0,x1
          move      #$0,y0
          move      #$0,y1
          bset      #4,omr              ; ebd
;
sbr       dor       #60,_end
          mac       x0,y0,a   x:(r0)+,x1          y:(r4)+,y1
          mac       x1,y1,a   x:(r0)+,x0          y:(r4)+,y0
          add       a,b
          mac       x0,y0,a   x:(r0)+,x1
          mac       x1,y1,a                       y:(r4)+,y0
          move      b1,x:$ff
_end
          bra       sbr
          nop
          nop
          nop
          nop
PROG_END
          nop
          nop


XDAT_START
;         org       x:0
          dc        $262EB9
          dc        $86F2FE
          dc        $E56A5F
```

```
dc        $616CAC
dc        $8FFD75
dc        $9210A
dc        $A06D7B
dc        $CEA798
dc        $8DFBF1
dc        $A063D6
dc        $6C6657
dc        $C2A544
dc        $A3662D
dc        $A4E762
dc        $84F0F3
dc        $E6F1B0
dc        $B3829
dc        $8BF7AE
dc        $63A94F
dc        $EF78DC
dc        $242DE5
dc        $A3E0BA
dc        $EBAB6B
dc        $8726C8
dc        $CA361
dc        $2F6E86
dc        $A57347
dc        $4BE774
dc        $8F349D
dc        $A1ED12
dc        $4BFCE3
dc        $EA26E0
dc        $CD7D99
dc        $4BA85E
dc        $27A43F
dc        $A8B10C
dc        $D3A55
dc        $25EC6A
dc        $2A255B
dc        $A5F1F8
dc        $2426D1
dc        $AE6536
dc        $CBBC37
dc        $6235A4
dc        $37F0D
dc        $63BEC2
dc        $A5E4D3
dc        $8CE810
dc        $3FF09
dc        $60E50E
dc        $CFFB2F
dc        $40753C
dc        $8262C5
dc        $CA641A
dc        $EB3B4B
dc        $2DA928
dc        $AB6641
dc        $28A7E6
```

```
          dc        $4E2127
          dc        $482FD4
          dc        $7257D
          dc        $E53C72
          dc        $1A8C3
          dc        $E27540
XDAT_END

YDAT_START
;         org       y:0
          dc        $5B6DA
          dc        $C3F70B
          dc        $6A39E8
          dc        $81E801
          dc        $C666A6
          dc        $46F8E7
          dc        $AAEC94
          dc        $24233D
          dc        $802732
          dc        $2E3C83
          dc        $A43E00
          dc        $C2B639
          dc        $85A47E
          dc        $ABFDDF
          dc        $F3A2C
          dc        $2D7CF5
          dc        $E16A8A
          dc        $ECB8FB
          dc        $4BED18
          dc        $43F371
          dc        $83A556
          dc        $E1E9D7
          dc        $ACA2C4
          dc        $8135AD
          dc        $2CE0E2
          dc        $8F2C73
          dc        $432730
          dc        $A87FA9
          dc        $4A292E
          dc        $A63CCF
          dc        $6BA65C
          dc        $E06D65
          dc        $1AA3A
          dc        $A1B6EB
          dc        $48AC48
          dc        $EF7AE1
          dc        $6E3006
          dc        $62F6C7
          dc        $6064F4
          dc        $87E41D
          dc        $CB2692
          dc        $2C3863
          dc        $C6BC60
          dc        $43A519
          dc        $6139DE
```

```
            dc      $ADF7BF
            dc      $4B3E8C
            dc      $6079D5
            dc      $E0F5EA
            dc      $8230DB
            dc      $A3B778
            dc      $2BFE51
            dc      $E0A6B6
            dc      $68FFB7
            dc      $28F324
            dc      $8F2E8D
            dc      $667842
            dc      $83E053
            dc      $A1FD90
            dc      $6B2689
            dc      $85B68E
            dc      $622EAF
            dc      $6162BC
            dc      $E4A245
YDAT_END
```

NOTES

How to Reach Us:

Home Page:
www.freescale.com

E-mail:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064, Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

***For Literature Requests Only*:**
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405

Document Number: DSP56366
Rev. 3.1
1/2007

freescale™
semiconductor